Course Code: 19EEEC201 **Course Title: Circuit Analysis**

L-T-P-SS: 4-0-0 **Credits: 4** **Contact Hrs: 50**

CIE Marks: 50 **SEE Marks: 50** **Total Marks: 100**

Teaching Hrs: 50 **Exam Duration: 3 hrs**

Chapter No.	Unit-I	Hrs
1	**Network Equations :**Source Transformation, Star Delta transformation, Nodal Analysis, Super node, Mesh Analysis, Super mesh, Duality, Network Topology, Tie Set and Cut Set matrix formulation, Dot convention.	8 hrs
2	**Network Theorems :**Homogeneity, Superposition and Linearity, Thevenin's & Norton's Theorems, Maximum Power Transfer Theorem, Milman's theorem, Reciprocity principle, Application of theorems to both ac and dc networks	8 hrs
3	**Two Port Networks :**Two port variables, Z,Y, H,G, A- Parameter representations, Input and output impedance calculation, Series, Parallel and Cascade network connections, and their (suitable) models.	4 hrs
	Unit-II	
4	**First order circuits :**Order of a system, Concept of Time constant, System Governing equation, System Characteristic equation, Basic RL & RC circuit, Transient response with initial conditions , Frequency response characteristics, R-C , R-L circuits as differentiator and integrator models, time and frequency domain responses R-C , R-L circuits as Low pass and high pass filters	8 hrs
5	**Higher order circuits:** Higher order R-C, R-L, and R-L-C networks, time domain and frequency domain representation, Series R-L-C circuit, Transient response, Damping factor, Quality factor, Frequency response curve , Peaking of frequency curve and its relation to damping factor, Resonance Parallel, R-L-C circuit, Tank circuit, Resonance, Quality factor and Bandwidth	12 hrs
	Unit-III	
6	**Sinusoidal Steady state analysis :** Characteristics of sinusoids, Forced response to sinusoidal functions, The complex forcing function, Phasors & Phasor diagrams.	5 hrs
7	**Polyphase Circuits :** Polyphase systems, Single Phase three wire system, Three phase Y-Y connection, Delta connection, Analysis of balanced & unbalanced three phase circuits.	5 hrs

Text Books

1 W H Hayt, J E Kemmerly, S M Durban, Engineering Circuit Analysis, 6th, McGraw Hil, 2006
2 M E. Van Valkenburg, Network Analysis, 3rd, Pearson Ed, 2006

Reference Books:

1 Joseph Edminister, Mahmood Nahavi, Electric Circuits, 3rd, Tata McGra, 1991
2 Bruce Carlson, Circuits, 3rd, Thomson Le, 2002
3 V. K. Aatre, Network Theory and Filter Design, 2nd, Wiley West, 2002
4 Anant Agarwal and Jeffrey H Lang, Foundations of Analog & Digital Electronics Circuits, 3rd, Morgan Kau, 2006
5 Muhammad H . Rashid, Introduction to PSPICE using OrCAD for circuits and Electronics, 3rd, Pearson Ed, 2005

Course Title: Analog Electronic Circuits **Course Code:15EEEC202**
L-T-P-SS: 4-0-0 **Credits: 4** **Contact Hours: 4Hrs/week**
CIE Marks: 50 **SEE Marks: 50** **Total Marks: 100**
Teaching Hours: 50Hrs **Examination Duration: 3Hrs**

Unit I	
Chapter 1: Applications of a Junction diode: Recap of piece-wise linear model, constant voltage drop model, ideal diode model, small signal model. Applications of diodes as a Clipping circuit and clamping circuits Voltage doubler.	06Hrs
Chapter 2: MOSFETs structure and physical operation: Device structure, operation with no gate voltage, creating a channel for current flow, applying small vds, operation as vds is increased, derivation of the id-vds relationship, the P-channel mosfet, complementary mos or cmos, operating the mos transistor in the sub threshold region. Current-voltage characteristics: circuit symbol, the id vs vds characteristics, finite output resistance in saturation, characteristics of the p-channel mosfet, the role of the substrate-the body effect, temperature effects, breakdown and input protection. MOSFET circuits at DC.	12 Hrs
Unit II	
Chapter 3:Current mirrors Basic current mirror, Widlar, Cascode and Wilson : Output impedance and Voltage swing.	08 Hrs
Chapter 4: MOSFET amplifiers : Biasing in MOS amplifier circuits, small signal operation and models, single stage mos amplifiers, the MOSFET internal capacitance and high frequency model, frequency response of CS amplifier.(CD and CG), Cascode Connection: Implications on gain and Bandwidth	12 Hrs
Unit III	
Chapter 5: Feedback Amplifiers : General feedback structure (Block schematic), Feedback desensitivity factor, positive and negative feedback Nyquist stability Criterion, RC phase shift oscillator, wein bridge oscillator, merits of negative feedback, feedback topologies: series-shunt feedback amplifier, series-series feedback amplifier, and shunt-shunt and shunt-series feedback amplifier with examples	06 Hrs
Chapter 6: Large Signal Amplifiers : Classification of amplifiers: (A, B, AB and C); Transformer coupled amplifier, push-pull amplifier Transistor case and heat sink.	06 Hrs

Text Books

1. A.S. Sedra & K.C. Smith, "Microelectronic Circuits", 5th Edition, Oxford Univ. Press, 1999.
2. Jacob Millman and Christos Halkias, “Integrated Electronics”, McGraw Hill,

References

1. David A. Bell, “Electronic Devices and Circuits” 4th edition , PHI publication 2007.
2. Grey, Hurst, Lewis and Meyer, “Analysis and design of analog integrated circuits,” 4th edition.
3. Thomas L. Floyd, “Electronic devices”, Pearson Education, 2002
4. Richard R. Spencer & Mohammed S. Ghousi, “ Introduction to Electronic Circuit Design”, Pearson Education, 2003
5. J. Millman & A. Grabel, "Microelectronics"-2nd edition, McGraw Hill, 1987.
6. Behzad Razavi, “Fundamentals of Microelectronics”, reprint 2015 Wiley publications.

Course Code: 19EEEC203 **Course Title: Digital Circuits**

L-T-P-Self Study: 4-0-0 **Credits: 4** **Contact Hrs: 50**

ISA Marks: 50 **ESA Marks: 50** **Total Marks: 100**

Teaching Hrs: 50 **Exam Duration: 3 hrs**

Content	Hrs
Unit – 1	
Chapter No. 1. Logic Families Logic levels, output switching times, fan-in and fan-out, comparison of logic families	2 hrs
Chapter No. 2.Principles of Combinational Logic Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4 variables, Incompletely specified functions(Don't care terms),Simplifying Maxterm equations, Quine-McCluskey minimization technique- QuineMcCluskey using don't care terms, Reduced Prime Implicant Tables.	8 hrs
Chapter No. 3.Analysis and design of combinational logic General approach, Decoders-BCD decoders, Encoders, Digital multiplexers- Using multiplexers as Boolean function generators. Adders and subtractors-Cascading full adders, Look ahead carry adders, Binary comparators.	10 hrs
Unit – 2	
Chapter No. 4.Introduction to Sequential Circuits Basic Bistable Element, Latches, A SR Latch, Application of SR Latch, A Switch De bouncer, The SR Latch, The gated SR Latch, The gated D Latch, The Master-Slave FlipFlops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop, Edge Triggered Flip-Flop: The Positive Edge-Triggered D Flip-Flop, Negative- Edge Triggered D Flip-Flop; Characteristic Equations	10 hrs
Chapter No. 5. Analysis of Sequential Circuits Registers and Counters, Binary Ripple Counters, Synchronous Binary counters, Ring and Johnson Counters, Design of a Synchronous counters, Design of a Synchronous Mod-n Counter using clocked JK Flip-Flops Design of a Synchronous Mod-n Counter using clocked D, T or SR Flip-Flops.	10 hrs
Unit – 3	
Chapter No. 6. Sequential Circuit Design Introduction to Sequential Circuit Design, Mealy and Moore Models, State Machine notations, Synchronous Sequential Circuit Analysis, Construction of state Diagrams and counter design.	5 hrs

Chapter No. 7. Introduction to memories Introduction and role of memory in a computer system, memory types and terminology, Read Only memory, MROM, PROM, EPROM, EEPROM, Random access memory, SRAM, DRAM, NVRAM.	5 hrs

Text Books (List of books as mentioned in the approved syllabus)

1. Donald D Givone, Digital Principles and Design, Tata McGraw Hill, 2002
2. John M Yarbrough, Digital Logic Applications and Design, Thomson Learning, 2001
3. A Anand Kumar, Fundamentals of Digital Circuits, PHI, 2003

References

1. Charles H Roth, Fundamentals pf Logic Design, Thomson Learning, 2004
2. R.D.Sudhaker Samuel, Logic Design, Sanguine Technical Publishers, 2005
3. R P Jain, Modern Digital Electronics, Tata McGraw, 2000

Course Code: 19EEEC202

Course Title: Electrical Power Generation, Transmission & Distribution

L-T-P-Self Study: 3-0-0-0 **Credits: 3** **Contact Hrs: 40**

ISA Marks: 50 **ESA Marks: 50** **Total Marks: 100**

Teaching Hrs: 40 **Exam Duration: 3 hrs**

Content	Hrs
Unit - 1	
Chapter No. 1. Generating Stations. selection of Site, Classification, General arrangement and operation of Hydroelectric plant with components, General arrangement and operation of Thermal power plant with components, General arrangement and operation of Nuclear power plant with components, Safety of Nuclear power reactor, storing and processing of spent fuel.	5 hrs
Chapter No. 2. Substations and Economic operations Sub stations : Types, Bus-bar arrangement Schemes, location and substation equipment's Economics :Important terms and curves commonly used in system operation, effect of Voltage and frequency on loads , Scheduling of generators, Choice of size and number of generator units, Interconnection of power stations	5 hrs
Chapter No. 3.Typical Transmission & distribution systems Introduction, electric supply system, comparison of AC and DC systems, Standard Voltages of Transmission & Distribution. . Advantages of High Voltage Power Transmission. (effect of increase in voltage on weight of conductor, Line Efficiency & Line Voltage Drop) Feeders, Distributors & Service Mains. Conductor types.	2 hrs
Chapter No. 4. Overhead Transmission Line (Mechanical Design) Overhead transmission lines: introduction, components of a typical OH system. Line supports & placing of the conductors, single phase and three phase systems. Single circuit and double circuit.. Spacing of conductors, Length of span & Sag in OH lines. Sag calculation in conductors. (a) Suspended on level supports. (b) Supports at different levels. Effect of wind and ice. Tension and sag at erection. Corona Phenomena & Factors affecting corona in OH lines Expressions for Critical disruptive & visual critical voltage. and corona power loss	3 hrs
Unit - 2	
Chapter No. 5. Line parameters (Electrical Design) Introduction to transmission line constants i.e. Resistance, Inductance and capacitance . Distributed resistance of the transmission line, skin effect and proximity effect. Inductance of the single phase & three phase lines. Inductance calculation with equilateral and unsymmetrical spacing of the lines. Transposition of line conductors. Capacitance for single phase & three phase lines. Effect of earth on capacitance of the line. Numerical solutions on resistance calculations. Inductance & Capacitance calculations.	7 hrs
Chapter No. 6. Characteristics & Performance of Power transmission lines:	8 hrs

Introduction to Short transmission lines, calculations for short lines. Medium transmission lines. Nominal-T and □ representation for transmission lines Long transmission lines. Long line solutions by Rigorous method, equivalent models, ABCD constants. .	
Unit - 3	
Chapter No. 7. Insulators Materials of insulators. Different types of insulators. Potential distribution over a string of suspension insulators. String efficiency and methods of increasing string efficiency. Testing of insulators.	5 hrs
Chapter No. 8. Underground Cables Underground Cables: Types of cables & material used for Insulation. Resistance, thermal rating of cables & charging current, Grading of cables Capacitance grading and inter sheath grading, testing of cables.	5 hrs

Text Books

1. Skrotzki and Wavopat, Power station Engineering and economics ., McGraw Hill, 1995

References

1. Soni, Gupta and Bhatnagar, A Course in Electrical Power, Dhanpatrai, 2014
2. S M Singh, Electric Power generation , transmission and Distribution., Prentice Hall of India., 2012
3. J B Gupta., Transmission and Distribution of Electrical power., Kataria, 2012

V K Metha and Rohit Metha., Principles of Power System., S Chand & Company Ltd.,

Course Title: Microcontroller Architecture & Programming **Course Code: 15EEEP201**

L-T-P: 0-1-1 **Credits: 2** **Contact Hours: 4Hrs/week**

CIE Marks: 80 **SEE Marks:20** **Total Marks: 100**

Teaching + Lab. Hours: 48Hrs **Examination Duration:3 Hrs**

1.	**Overview of Architecture of 8051:** • Processor Core and Functional Block Diagram • Description of memory organization • Overview of ALL SFR's and their basic functionality	02+02 Hrs
2.	**Low Level programming Concepts:** • Addressing Modes • Instruction Set and Assembly Language programming(ALP) • Developing, Building, and Debugging ALP's	02+02 Hrs
3.	**Middle Level Programming Concepts:** • Cross Compiler • Embedded C language implementation, programming, & debugging • Differences from ANSI-C • Memory Models • Library reference • Use of directives • Functions, Parameter passing and return types	04+04Hrs
4.	**On-Chip Peripherals Study,Programming, and Application:** • Ports: Input/Output • Timers & Counters • UART • Interrupts	04+04Hrs
5.	**External Interfaces Study,Programming and Applications :** • LEDS • Switches(Momentary type, Toggle type) • Seven Segment Display: (Normal mode, BCD mode,Internal Multiplexing & External Multiplexing) • LCD (8bit, 4bit, Busy flag, custom character generation) • Keypad Matrix	04+04Hrs
6.	**Selective Discussion during Project Development** • A/D & D/A Converter • Stepper Motor, DC Motor • ZIGBEE • GSM/GPS • USB • MMC & SD • Ethernet MAC	08+08Hrs

Text Book*Text Books:*

1. Kenneth J. Ayala ; "The 8051 Microcontroller Architecture, Programming & Applications" 2e, Penram International, 1996 / Thomson Learning 2005
2. Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; "The 8051 Microcontroller and Embedded Systems – using assembly and C "- PHI, 2006 / Pearson, 2006

References Books:

1. Predko ; "Programming and Customizing the 8051 Microcontroller" –, TMH
2. Raj Kamal, "Microcontrollers: Architecture, Programming, Interfacing and System Design", Pearson Education, 2005
3. Ajay V.Deshmukh; "Microcontrollers- Theory and Applications",TMH,2005
4. Dr.RamaniKalpathi and Ganesh Raja; "Microcontroller and its applications", Sanguine Technical publishers,Bangalore-2005

Course Title: Digital Electronics Laboratory **Course Code: 15EEEP203**

L-T-P: 0-0-1 **Credits: 1** **Contact Hours: 2Hrs/week**

CIE Marks: 80 **SEE Marks: 20** **Total Marks: 100**

Laboratory Hours: 28Hrs **Examination Duration: 3Hrs**

List of Experiments:

1. Characterization of TTL & CMOS Gates– Propagation delay, Fan-in, Fan-out and Noise Margin.
2. Design and implement binary to gray, gray to binary, BCD to Ex-3 and Ex-3 to BCD code converters.
3. Design and implement BCD adder and Subtractor using 4 bit parallel adder.
4. Design and implement given functionality using decoders and multiplexers.
5. Design and implement n bit magnitude comparator using 4- bit comparators.
6. Design and implement Ring and Johnson counter using shift register.
7. Design and implement mod-6 synchronous and asynchronous counters using flip flops.
8. Design and implement a digital system to display a 3 bit counter on a 7 segment display. Demonstrate the results on a general purpose PCB.
9. Design and implement 1-bit serial adder. Demonstrate the results on a general purpose PCB.

Reference Books

1. Books/References: 1. K.A.Krishnamurthy “Digital lab primer”, Pearson Education Asia Publications, 2003.
2. **“**Electronic Principles” by A.P. Malvino, TaTa MGH,5th ED

Course Title: Analog Electronics Laboratory **Course Code: 15EEEP202**

L-T-P: 0-0-1 **Credits: 1** **Contact Hours: 2Hrs/week**

CIE Marks: 80 **SEE Marks: 20** **Total Marks: 100**

Laboratory Hours: 28Hrs **Examination Duration: 3Hrs**

List of Experiments:

1. Design &Testing of Diode Clipping (single/double ended) circuits
2. Design &Testing of Clamping circuits for Positive and Negative Clamping.
3. Design of RC Coupled single stage FET/BJT amplifier &determination of the gain – frequency response, I/P & O/P impedance.
4. MOSFET characteristics
5. Design of single stage CS (MOSFET) amplifier &determination of the gain – frequency response.
6. Design of source follower using MOSFET.
7. Design and testing Current mirror circuit MOSFET
8. Design of two stage voltage series feed-back amplifier & determination of the gain, frequency response, i/p &o/p impedance with &without feedback
9. Design and testing of Transformer-less push-pull class B power amplifier
10. Design of Darlington Emitter follower with and without Bootstrapping and determines the gain, i/p and o/p impedance.

Reference Books

1. **"**Electronic Devices & circuit Theory " by Nashelsky & Boylstead,PHI,9th Ed
2. "Integrated Electronics" By 'Jacob Millman and Christos Halkias',McGraw Hill,
3. **"**Electronic Principles" by A.P. Malvino, TaTa MGH,5th Ed

Course Code: 19EEEC204 **Course Title: Electrical Machines**
L-T-P : 4-0-0 **Credits: 3** **Contact Hrs: 50**
ISA Marks: 50 **ESA Marks: 50** **Total Marks: 100**
Teaching Hrs: 50 **Exam Duration: 3Hrs**

Content	Hrs
Unit – 1	
Chapter 1: Transformers: Single phase transformer- Principle of operation and construction, Ideal transformer, Real transformer, Phasor diagrams, Equivalent circuit, Open-circuit test, Short-circuit test, Voltage regulation, Efficiency, Three phase transformers.	**09 hours**
Chapter 2: Three Phase Induction Machines: Principle of energy conversion in machines, Construction, Fundamental relationships- Slip, Rotor speed, Input power, Electromagnetic power, Electromagnetic (developed) torque, Mechanical power, Efficiency, Shaft torque. , Equivalent circuit, Analogies between induction machine and transformer, No-load and locked-rotor tests, Torque-speed characteristics, Starting, Speed control. Inverter fed induction motor.	**11 hours**
Unit – 2	
Chapter 3: DC Machines: Principle of operation, Construction of DC machine, Fundamental equations, Armature reaction, Classification of DC machines, DC generators, DC motors, Starting, Speed control of DC motors ,Braking, Switched Reluctance Machines-Construction, principle of operation , Aligned and unaligned positions, Electromagnetic torque, Advantages, disadvantages and Applications of SRMs, Steady state analysis of SRM. BLDC motor Construction and operation.	**12 hours**
Chapter 4: Synchronous Machines: Construction, Classification of synchronous machines, Electromotive force induced in armature winding, Generator and motor operation, Phasor diagrams of synchronous machine with Non-salient pole rotor and salient pole rotor, Voltage regulation calculation by EMF and MMF method, Synchronous motor, Synchronous motor as a synchronous condenser, Study of V and inverted V curves.	**08 hours**
Unit – 3	
Chapter 5: Synchronous Machines: Permanent magnet synchronous motors, Air gap magnetic flux density, Equivalent circuit of PM synchronous machine, Phasor diagram, Performance Characteristics of PM synchronous machine, Starting.	**05 hours**
Chapter 6: Single phase induction motors: Double revolving field theory, Equivalent circuit, Split-phase induction motor, Capacitor-start induction motor, Permanent split capacitor induction motor, Capacitor start capacitor-run induction motor, and Shaded pole induction motor.	**05 hours**

Text Book

1. Jacek F. Gieras, "Electrical Machines: Fundamentals of Electromechanical Energy Conversion", CRC Press, Taylor & Francis Group, 2017.

References

1. P. C. Sen, "Principles of Electric Machines and Power Electronics", John Wiley & Sons Publications, Canada, 2nd Edition, 2001.

2. Bhimbra, “Principles of Electrical machinery”, Khanna Publishers.2006.
3. Mehrdad Ehsani…[et al.],“Modern electric, Hybrid electric, and Fuel Cell Vehicles: fundamentals, theory, and design.”, CRC Press, 2005.
4. T. J. E.Miller, “Brushless Permanent-Magnet and Reluctance Motor Drives”, Oxford Science Publications, 1989.

Course Code: 17EEEC204 **Course Title: Linear Control Systems**

L-T-P: 3-0-0 Credits: 3 Contact Hrs: 40

ISA Marks: 50 ESA Marks: 50 Total Marks: 100

Teaching Hrs: 50 Exam Duration: 3 hrs

Chapter No.	Unit-I	
1	**Introduction to control systems**: Open loop and closed loop control systems-definitions, salient features and simple examples	2 Hrs
2	**Transfer function Models and block diagram representation:** Definition of transfer function, assumptions and properties, Block diagram and signal flow graph representation**,** symbols used. Block-diagram of negative and positive feedback systems. Electrical systems: Derivation of transfer functions for electrical circuits, Models of dc servomotors-armature and field control, block-diagram representation. Block diagram reduction rules, Examples.	6 Hrs
3	**Time Response Analysis** Poles and Zeros, Type and order, Standard test signals. First order system: unit step response, importance of time constant, Second order system: Standard T.F of second order system. Unit step response of 2^{nd} order system Time response specifications-definition. Expressions for rise time, peak time, peak overshot and settling time, Static error constants and steady-state errors.	7 Hrs
	Unit-II	
4	**Stability Analysis of control systems:** Explanation of Routh-Hurwitz criterion-necessary and sufficient condition for stability, special cases, Absolute and Relative stability, relative stability analysis.	5 Hrs
5	**Controller design approaches:** Basic modes of controls and their features: On-Off, proportional, integral, PI, PD and PID, Controller design approaches- Zeigler Nichol's tuning method and Pole placement design method, design examples	5 Hrs
6	**Frequency response analysis:** Sinusoidal response: system response for sinusoidal inputs**,** sinusoidal transfer functions. Frequency response of a second order system, definitions and expressions of Frequency response specifications. Polar plot: method to draw approximate polar plot, definition of phase and gain margin.	5 Hrs
	Unit-III	
7	**Bode plot analysis of control systems:** Bode plots: asymptotic plots for basic factors, method to draw Bode asymptotic plot and phase plot, determination of gain and phase margins from Bode plot.	5 Hrs
8	**Root locus diagrams:** Basic principle – magnitude and angle criterion, Rules to construct root locus diagram (proof not required), method to construct root locus diagram.	5 Hrs

Text Books

1 Nagarath and Gopal, *Control system Engineering,* Wiley Eastern Ltd., 1995, 2^{nd} edition.

2 Katsuhiko Ogata, *Modern Control Engineering,* PHI, 2002, 4^{th} edition

Reference Books:

1 M.Gopal, Control Systems-Principles and Design, 2, TMH, 2002.

Course Code: **15EEEC207** Course Title: **ARM Processor & Applications**
L-T-P-SS: **4-0-0-0** Credits: **4** Contact Hours:**4 Hrs/week**
CIE Marks: **50** SEE Marks:**50** Total Marks: **100**
Teaching Hours:**50Hrs** Examination Duration:**3Hrs**

Content	Hrs
Unit - 1	
Chapter No.1 Interrupt programming 8051-Interrupts and programming (both assembly and 'C'): Interrupts for timer and serial communication.	5 hrs
Chapter No.2 ARM Architecture The Acorn RISC machine, Architectural inheritance, Architecture of ARM7TDMI, ARM programmers model, ARM development tools, 3 stage pipeline ARM organization, ARM instruction execution.	5 hrs
Chapter No.3 Introduction to ARM instruction set Data processing instruction, Branch instruction, Load store instruction, Software interrupt instruction, Program status register instruction, Conditional execution, Example programs.	5 hrs
Unit - 2	
Chapter No.4 Introduction to THUMB instruction set The Thumb programmer model, ARM-Thumb interworking, other branch instructions, Data processing instructions, Single/Multiple register load store instruction, Stack operation, Software interrupt instructions, example programs.	2 hrs
Chapter No.5 Assembler rules and Directives Introduction, structure of assembly language modules, Predefined register names, frequently used directives, Macros, Miscellaneous assembler features. Example programs.	4 hrs
Chapter No.6 Exception handling Introduction, Interrupts, error conditions, processor exception sequence, the vector table, Exception handlers, Exception priorities, Procedures for handling exceptions.	4 hrs
Chapter No.7 Architectural support for high level languages Abstraction in software design, data types, floating point data types, The ARM floating point architecture, use of memory, run time environment.	5 hrs
Unit - 3	
Chapter No.8 LPC2148 Architecture and applications On-chip memory, GPIOs, Timers, UART, ADC, I2C, SPI , RTC, ARM interfacing techniques and programming: LED, LCD, Stepper Motor, Buzzer, Keypad, ADC and I2C	10 hrs

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Text Books (List of books as mentioned in the approved syllabus)

1.	Steve Furber, ARM System- on-Chip Architecture, 2nd, LPE, 2002
2.	William Hohl, ARM Assembly Language fundamentals and Techniques, 1st, CRC press, 2009

References

- "ARM system Developer's Guide"- Hardbound, Publication date: 2004 Imprint: MORGAN KAUFFMAN
- User manual on LPC21XX.

Course Title: ARM Microcontroller Lab **Course Code: 15EEEP205**
L-T-P: 0-0-1 **Credits: 1** **Contact Hours: 2Hrs/week**
CIE Marks: 80 **SEE Marks: 20** **Total Marks: 100**
Teaching Hours: 25Hrs **Examination Duration: 2 Hrs**

Chapter No.	List of Experiments
1	Write an ALP to achieve the following arithmetic operations: i. 32 bit addition ii. 64 bit addition iii. Subtraction iv. Multiplication v. 32 bit binary divide
2	Write an ALP for the following using loops: i. Find the sum of 'N' 16 bit numbers ii. Find the maximum/minimum of N numbers iii. Find the factorial of a given number with and without look up table.
3	Write an ALP to i. Find the length of the carriage r1eturn terminated string. ii. Compare two strings for equality. ii.
4	Write an ALP to pass parameters to a subroutine to find the factorial of a number or prime number generation.
5	Write a 'C' program to test working of LED's using LPC2148.
6	Write a 'C' program & demonstrate an interfacing of Alphanumeric LCD 2X16 panel to LPC2148 Microcontroller.
7	Write an ALP to generate the following waveforms of different frequencies i. Square wave ii. Triangular iii. Sine wave II.Write a 'C' program & demonstrate interfacing of buzzer to LPC2148(using external interrupt)
8	Write a program to set up communication between 2 microcontrollers using I2C.
9	Write a 'C' program & demonstrate an interfacing of ADC.
Structured Enquiry	
1	Write a program that displays a value of 'Y' at port 0 and 'N' at port 2 and also generates a square wave of 10Khz with Timer 0 in mode 2 at port pin p1.2 XTAL =22MHz
2	Write a C program that continuously gets a single bit of data from P1.7 and sends it to P1.0 in main, while simultaneously i. creating a square wave of 200us period on pin P2.5. ii. Sending letter 'A' to serial port. Use Timer 0to create square wave.
Open Ended	
1	Develop an ARM based application using i. sensors ii. Actuators iii. displays

Course Title: Digital System Design using Verilog **Course Code: 18EEEP203**
L-T-P: 0-0-2 **Credits: 2** **Contact Hours: 4Hrs/week**
ISA Marks: 80 **SEA Marks:20** **Total Marks: 100**
Teaching + Lab. Hours: 48 Hrs **Examination Duration: 2 Hrs**

1.	Chapter No. 1. Architecture of FPGA Architecture of FPGS: Spartan 3, What Is HDL, Verilog HDL Data Types and Operators.	4hrs
2.	Chapter No. 2. Data Flow Descriptions Highlights of Data-Flow Descriptions, Structure of Data-Flow Description, Data Type – Vectors, Testbench.	6 hrs
3.	Chapter No. 3. Behavioral Descriptions Behavioral Description highlights, structure of HDL behavioral Description, The VHDL variable –Assignment Statement, sequential statements, Tasks and Functions	10 hrs
4.	Chapter No. 4. Structural Descriptions Highlights of structural Description, Organization of the structural Descriptions, Binding, state Machines, Generate, Generic, and Parameter statements	10 hrs
5.	Chapter No. 5:Finite State Machine: Moore Machines, Mealy Machines	4hrs
6.	Chapter No. 6:Timing Issues in Digital Circuits: Setup Time Constraints, Hold Time Constraints, Static Time analysis, Critical Path, Clock Skew.	6hrs
7.	Chapter No. 7. Advanced HDL Descriptions File operations in Verilog, Memories: RAM, ROM, Block Memories(Xilinx IP)	8hrs

Course code: 17EEEC302
Course title: Power System Analysis & Stability **CIE Marks: 50**
Teaching hours: 40 **SEE Marks: 50**

Course Content	Hrs
Unit - 1	
Chapter No. 1: Power system representation Standard symbols of power system components, one-line diagram, impedance and reactance diagrams, per-unit quantity-definition, per-unit impedance of 3-phase component, change of base, equivalent load impedance, p.u impedance of two-winding transformer referred to primary and secondary, method to draw p.u impedance diagram, advantages of p.u system calculations, examples on obtaining per-unit reactance diagram and per-unit calculations	6 hrs
Chapter No. 2: Symmetrical fault analysis 3-Phase short circuit at the terminals of unloaded generator, definitions of sub-transient, transient and steady-state reactance, internal emf's of loaded machines, examples on short circuit calculations, selection of circuit breaker ratings-momentary current and interrupting capacity, examples on symmetrical fault calculations.	5 hrs
Chapter No. 3: Introduction to Symmetrical components and sequence networks Definition of sequence components as applied to 3-phase unbalanced systems, expressions for sequence components, examples on computations of sequence components.	4 hrs
Unit - 2	
Chapter No. 4 Sequence Networks Sequence impedance and sequence network, sequence networks of 3-phase generator, zero-sequence networks of 3-phase loads and transformers, Sequence network of power systems	4 hrs
Chapter No. 5: Unsymmetrical Fault Analysis Single line to ground, line to line and double line to ground fault with fault impedance at the terminals of unloaded generator- derivation of connection of sequence networks, Unsymmetrical faults on unloaded power systems, examples on unsymmetrical fault calculation for unloaded power systems.	7 hrs
Chapter No. 6: Introduction to power system Stability Power angle equation of SMIB system, steady-state analysis, M&H constants-definitions and relation, swing equation, equal area criterion (EAC),	4 hrs
Unit - 3	
Chapter No. 7: Stability analysis by EAC: EAC applications to to-sudden change in mechanical power input, 3-phase fault on transmission line, expression for critical clearing angle, examples on EAC applications	5 hrs
Chapter No. 8: Numerical solution of swing equation for stability analysis Point by point method of solving swing equation, applications of Euler, modified Euler and R-K numerical techniques for stability analysis, methods to improve transient stability, examples on stability analysis	5 hrs

Text Books

1. W.D. Stevenson, Elements of Power System Analysis, 4th Edition, McGraw Hill, 1982
2. I.J. Nagarath and D.P. Kothari, Power System Engineering, 2nd Edition, Tata McGraw Hill, 2010

Reference Books

1. Hadi Sadat, Power System Analysis, First Edition, Tata McGraw Hill, 2002
2. Nagarath and Kothari, Modern Power System Analysis, 2nd Edition, Tata McGraw Hill, 1993
3. J.J. Grainger and W.D. Stevenson, Power System Analysis, McGraw Hill (New York), 1994

Course Code: 21EEEC301	Course Title: Electric Drives & Control	
L-T-P-Self Study: 3-0-0	Credits: 3	Contact Hrs: 40
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3 hrs

Content	Hrs
Unit - 1	
Chapter No.1 :An introduction to Electrical Drives & its Dynamics Electrical drives. Advantages of electrical drives. Parts of electrical drives, Choice of electrical drives, status of dc and ac drives, Dynamics of electrical drives, Fundamental torque equation, speed torque conventions and multi quadrant operation. Nature and classification of load torques, calculation of time and energy loss in transient operations.	5 hrs
Chapter No.2: D C Motor Drives Starting braking, single phase fully controlled rectifier, control of dc separately excited motor, Single-phase half controlled rectifier control of dc separately excited motor. Three phase fully controlled rectifier control of dc separately excited motor, three phase half controlled rectifier control of dc separately excited motor, multi-quadrant operation of dc separately excited motor fed form fully controlled rectifier. Rectifier control of dc series motor, chopper controlled dc drives, chopper control of separately excited dc motor. Chopper control of series motor.	10 hrs
Unit - 2	
Chapter No. 3: Induction Motor Drives Operation with unbalanced source voltage and single phasing, operation with unbalanced rotor impedances, analysis of induction motor fed from non-sinusoidal voltage supply, starting, braking, stator voltage control, variable voltage, variable frequency control from voltage sources, voltage source inverter control, current source inverter control, current regulated voltage source inverter control, rotor resistance control, slip power recovery.	10 hrs
Chapter No. 4: Synchronous Motor and Brushless DC Motor Drives Operation from fixed frequency supply, synchronous motor variable speed drives, variable frequency control of multiple synchronous motors, self-controlled synchronous motor drive, PMAC motor drives, brushless dc motor drives.	5 hrs
Unit - 3	
Chapter No. 5:Stepper Motor and Switched Reluctance Motor Drives Stepper Motor: variable reluctance, permanent magnet, torque versus stepping rate characteristics drive circuits for stepper motors Switched Reluctance Motor: Operation and control requirements, converter circuits, modes of operation	5 hrs
Chapter No. 6: Solar and Battery Powered Drives Solar panels, motors suitable for pump drives, battery powered vehicles, solar powered electrical vehicles	5 hrs

Text Books (List of books as mentioned in the approved syllabus)

1. G. K Dubey, Fundamentals of Electrical Drives, 2, Narosa Publishing House, Chennai, 2002

References

1. N. K. De and P. K. Sen, Electrical Drives, PHI, 2007

2. S. K. Pillai, A First Course On Electric Drives, Wiley Eastern Ltd, 1990

3. V. R. Moorthi, Power Electronics, Devices, Circuits & Industrial Applications, Oxford University Press, 2005

Course Code: 17EEEC303 **Course Title: OS and Embedded Systems**
L-T-P-SS: 3-0-0 **Credits: 3** **Contact Hrs: 3 hrs/week**
CIE Marks: 40 SEE Marks: 50 **Total Marks: 100**
Teaching Hrs: 40 hrs **Exam Duration: 3 hrs**

No	Content	Hrs
1	**Unit I** **Introduction and System structures** Operating system definition; Operating System operations; Different types of operating system – Mainframe systems, Multi programmed systems, Time sharing systems, Desktop systems, Parallel systems, Distributed systems, Real time systems. **Process Management** Process concept; Process scheduling; Operations on processes; Inter-process communication. Multi-Threaded Programming: Overview; Multi threading models; Thread Libraries; Threading issues. Process Scheduling: Basic concepts; Scheduling criteria; Scheduling algorithms; Multiple-Processor scheduling; Thread scheduling. **Memory Management** Memory Management Strategies: Background; Swapping; Contiguous memory allocation; Paging; Structure of page table; Segmentation. Virtual Memory Management: Background; Demand paging; Page replacement; Allocation of frames; Thrashing. **(Textbook: Galvin)**	03 Hrs 06 Hrs **06 Hrs**
	Unit II	
4	**Introduction To Real-Time Operating Systems** Introduction To Real-Time Operating Systems: Introduction to OS, Introduction to real time embedded system- real time systems, characteristics of real time systems , the future of embedded systems. Introduction to RTOS, key characteristics of RTOS, its kernel, components in RTOS kernel, objects, scheduler, services, context switch, Scheduling types: Preemptive priority-based scheduling, Round-robin and preemptive scheduling. **Tasks, Semaphores and Message Queues:** Tasks, Semaphores and Message Queues: A task, its structure, A typical finite state machine, Steps showing the how FSM works. A semaphore, its structure, binary semaphore, mutual exclusion (mutex) semaphore, Synchronization between two tasks and multiple tasks, Single shared-resource-access synchronization, Recursive shared-resource-access synchronization. A message queue, its structure, Message copying and memory use for sending and receiving messages, Sending messages in FIFO or LIFO order, broadcasting messages. ***(Textbook: Qing Li with Caroline Yao, Real-Time Concepts for Embedded Systems, 1E, Published, 2011)***	08 Hrs 07 Hrs
3	**Unit III** **Typical Embedded System:** Classification and purposes of embedded system, Characters and Quality attributes of embedded system, Core and Supporting components of embedded system, Embedded firmware **(Text book: Shibu KV)** Wired and Wireless Protocols: **Bus communication protocol (USB,I^2C,SPI), Wireless and mobile system protocol (Bluetooth, 802.11 and its variants, ZigBee), Embedded design cycle-case study-ACVM** (Text book: Rajkamal)	05 Hrs **05 Hrs**

Course Code: 18EEEC301 **Course Title: Linear Integrated Circuits**

L-T-P: 3-0-0 Credits: 3 Contact Hrs: 40

CIE Marks: 50 SEE Marks: 50 Total Marks: 100

Teaching Hrs: 40 Exam Duration: 3 hrs

Chapter No.	Unit-I	
1	**Current Mirrors** Current Mirror circuits and Modeling, Figures of merit (output impedance, voltage swing), Widlar, Cascode and Wilson current Mirrors, Current source and current sink.	05 Hrs
2	**Basic OPAMP architecture** Basic differential amplifier, Common mode and difference mode gain, CMRR, 5-pack differential amplifier, 7-pack operational amplifier, Slew rate limitation, Instability and Compensation, Bandwidth and frequency response curve	06 Hrs
3	**OPAMP characteristics** Ideal and non-ideal OPAMP terminal characteristics, Input and output impedance, output Offset voltage, Small signal and Large signal bandwidth.	04 Hrs
	Unit-II	
4	**OPAMP with Feedback** OPAMP under Positive and Negative feedback, Impact Negative feedback on linearity, Offset voltage, Bandwidth, Input and Output impedances,Follower property, Inversion property	05Hrs
5	**Linear applications of OPAMP** DC and AC Amplifiers, Voltage Follower, Summing, Scaling and Averagingamplifiers (Inverting, Non-inverting and Differential configuration), Integrator, Differentiator, , Currentamplifiers, Instrumentation amplifier,Phase shifters, Voltage to current converter, Phase shift oscillator, Weinbridge oscillator, Active Filters –First and second order Low pass & High pass filters.	10 Hrs
	Unit-III	
6	**Nonlinear applications of OPAMP** Crossing detectors (ZCD. Comparator),Schmitt trigger circuits, Monostable & Astable multivibrator, Triangular/rectangular wave generators, Waveform generator, Voltage controlled Oscillator,Precisionrectifiers, Limiting circuits.Clamping circuits, Peak detectors, sample and hold circuits, Log and antilog amplifiers, Multiplier and divider Amplifiers, Voltage Regulators.	10 Hrs

Text Books

1 Sedra and Smith, “Microelectronics ”, 5th edition , Oxford University Press.

2 Ramakant A. Gayakwad, “Op - Amps and Linear Integrated Circuits”, 4th edition, PHI.

Reference Books:

1 Robert. F. Coughlin &Fredrick F. Driscoll, “Operational Amplifiers and Linear Integrated Circuits”, PHI/Pearson, 2006.

2 James M. Fiore, “Op - Amps and Linear Integrated Circuits”, Thomson Learning, 2001

3 Sergio Franco, “Design with Operational Amplifiers and Analog Integrated Circuits”, TMH, 3e, 2005

4 David A. Bell, “Operational Amplifiers and Linear IC’s”, 2nd edition, PHI/Pearson, 2004

Course code: 19EEEC301 **L-T-P: 2-0-1**
Course title: Machine Learning **CIE Marks: 50**
Teaching hours: 40 **ESA Marks: 50**

Chapter No.	Unit-I	
1	**Introduction** Introduction to Machine Learning, Applications of Machine Learning, Types of Machine Learning: Supervised, Unsupervised and Reinforcement learning, Dataset formats, Basic terminologies.	5 hrs
2	**Supervised Learning** Linear Regression, Logistic Regression Linear Regression: Single and Multiple variables, Sum of squares error function, The Gradient descent algorithm, Application, Logistic Regression, The cost function, Classification using logistic regression, one-vs-all classification using logistic regression, Regularization.	10 hrs
	Unit-II	
3	**Supervised Learning: Neural Network** Introduction to perception learning, Implementing simple gates XOR, AND, OR using neural network. Model representation, Gradient checking, Back propagation algorithm, Multi-class classification, Application- classifying digits, SVM.	10 hrs
4	**Unsupervised Learning: Clustering** Introduction, K means Clustering, Algorithm, Cost function, Application.	5 hrs
	Unit-III	
5	**Unsupervised Learning: Dimensionality Reduction** Dimensionality reduction, PCA- Principal Component Analysis. Applications, Clustering data and PCA.	4 hrs
6	**Introduction to Deep Learning** What is deep learning?, Difference between machine learning and deep learning, Convolution Neural Networks (CNN), Recurrent Neural Networks(RNN), When to use deep learning?	8 hrs

Text Books

1 Tom Mitchell, Machine Learning, 1, McGraw-Hill. , 1997
2 Christopher Bishop, Pattern Recognition and Machine Learning, 1, Springer, 2007

Reference Books:

1 Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning : Data Mining, Inference and Prediction, 2, Springer, 2009

Course Code: 17EEEP306 **Course Title: RTOS Lab**

L-T-P: 0-0-1 **Credits: 1** **Contact Hrs: 32**

CIE Marks: 20 **SEE Marks: 80** **Total Marks: 100**

Teaching Hrs: 32 **Exam Duration: 2 hrs**

Expt No.	List of Experiments
1	Write a C program to use on chip Timers in LPC2148 and generate required delay
2	Write a C program to demonstrate the concept of basic RTOS programming by using RTX RTOS
3	Write a 'C' program & demonstrate concept of Round Robin Task Scheduling.
	Write a C program to demonstrate the concept of basic preemptive scheduling algorithm by using RTX RTOS
4	Write a 'C' program & demonstrate concept of Events and Flags for inter task communication using RTX RTOS
5	Write a 'C' program & demonstrate concept of Mailbox.
6	Write a 'C' program & demonstrate concept of Semaphore.
7	Write a 'C' program & demonstrate concept of interrupts(hardware and software)
	Write a C program to interface I2C-RTC with LPC2148
8	Write a C program to interface SPI-EEPROM with LPC2148
	Structured Enquiry
9	Real-Time OS Application which successfully demonstrates the use of various RTOS concepts

Course Title: Machines lab **Course Code: 19EEEP301**

L-T-P: 0-0-1 **Credits: 1** **Contact Hours: 2Hrs/week**

CIE Marks: 80 **SEE Marks: 20** **Total Marks: 100**

Laboratory Hours: 28Hrs **Examination Duration: 3Hrs**

Category: Demonstration	
Expt./ Job No.	**Experiment / Job Details**
1	Star and Delta Connected Lighting Loads
2	Open circuit characteristics of DC machine
3	Speed control of separately excited DC motor by armature voltage control and flux control
4	Synchronization of Alternator with Bus bar/ Parallel operation of Alternator
Category: Exercise	
Expt./ Job No.	**Experiment / Job Details**
1	To Conduct NO – LOAD & BLOCKED ROTOR test on a given Induction motor to a) Find the performance parameters b) Represent the motor by its equivalent circuit model referred to Stator or Rotor.
2	To Conduct Open Circuit and Short Circuit test on given single phase transformer to a) Calculate efficiency and voltage regulation at different loads & power factors. b) Draw the transformer equivalent circuit model.
3	Load test on 3Ø Induction motor
4	Three phase Transformer bank using three single phase transformers with different configurations of primary and secondary windings.
5	Speed control of Induction motor by V/f method
6	Performance study of synchronous motor with change in its excitation (V and Inverted V curves)
7	Voltage regulation of an Alternator by EMF and MMF method
Category: Structured Enquiry	
Expt./ Job No.	**Experiment / Job Details**
1	To develop the second order response surface methodology (RSM) based speed prediction model of DC shunt motor by conducting experiments as per Design of Experiments.(DOE)

Course Title: Linear Integrated Circuits and Control System Lab		Course Code: 21EEEP301
L-T-P: 0-0-1	Credit:1	Contact Hours: 2hrs/week
CIE Marks:80	SEE Marks: 20	Total Marks:100
Laboratory Hours: 2hrs	Exam Duration:2 hrs	

Expt. No.	List of Experiments
	Demonstration
1.	Demonstration of Basic Op Amp Circuits
	Exercises
1.	Design and implementation of Rectifier Circuits
2.	Design and implementation of Wave shaping circuits (clippers and clampers)
3.	Design and implementation of Filter circuits (LPF and HPF)
4.	Design and implementation of waveform generating circuits (Schmitt trigger and Zero Crossing Detector)
5.	Design and simulation of Data converter circuits (R-2R D-A Converter)
6.	Design and analyze time response specifications of second order system
7.	Design and analyze frequency response specifications of second order system
8.	Design and analyze Lag and Lead Compensators
	Structured Enquiry
1.	Simulate and Investigate the effect of P, PI, PID controllers on the time response of a given second order series RLC system.

Books:

1. Op amps and Linear Integrated Circuits by Ramakant A. Gayakwad
2. Nagarath and Gopal, Control System Engineering, 2, Wiley-Eastern Limited, 1995.
3. K. Ogata, Modern Control Engineering, 4th Edition, PHI, 2002.

References:

1. Op-amps and Linear ICs by Prof. B.N. Yoganarasimhan
2. M. Gopal, Control Systems-Principles and Design, 2, TMH, 2002.

Course Code: 17EEEW301 **Title: Mini Project**
L-T-P: 0-0-3 Credits:3 **Contact Hrs: 3 hrs/week**
CIE Marks: 50 SEE Marks: 50 **Total Marks: 100**

Students are supposed to carry out the mini project based on the theme and guidelines as given below.

(I) Theme: A Computer Aided Solution to Electrical Engineering Problems

1. The work must involve designing and developing a computer solution to an electrical engineering problem with the help of a computer program written in C/C++.
2. Computer program must make use of data structures /algorithms suitable to the problem being solved.
3. The solution must involve mathematical modeling, mathematical solution and numerical methods.
4. Computer program design must be well documented through flowcharts.
5. Computer program must have a user manual and source code documentation.
6. Computer program must generate a clear, concise report that is useful for other users.
7. The solution must be documented in a report consisting of problem definition, methodology, modeling, solution, results and discussion and conclusions.

(II) Project batches and Guide:
Each project batch consists of 3 or 4 students. Students are informed to form their own batch based on the kind of project work and their interest. Each batch is supposed to give four faculty names as guides in the order of their preference. Guides will be allocated based on the preference given by the batch. The primary role of the guide is to supervise the work, provide appropriate guidance in successfully carrying out the project work.

(III) Project implementation
The principle steps in carrying out the project work are summarized below:
Step-1: Literature survey:
A literature survey with regard to the given theme is to be carried out in order to understand the state of the current research. Further, a critical review of the collected literature will facilitate to summarize key observations. Key observations will lead to identifying a specific problem for the project work in terms of alternate/new solution techniques, possible improvements, new formulations or models, hardware implementations etc.

Step-2: Prepare a synopsis:
A synopsis highlights the definition of identified problem and its significance. The synopsis will also contain detailed literature review giving the state of the current research on the selected specialized area.

It will also brief the problem formulation, solution methodology, tools employed and possible outcomes.

Step-3: Project implementation:

The work is to be carried out in phase wise manner, testing or analyzing the partial results obtained. Guide will periodically monitor the progress of the work done giving suitable suggestions as required.

(IV) Schedule:

Sl. No.	Activity	Week No.	Evaluation Objectives
1	Announcement for the formation of batches	At the end of the previous semester	NA
2	Allotment of guides	1st - 2nd	NA
3	Submission of Synopsis	3rd - 5th	Literature review, problem formulation, solution methodology, tools employed
4	Review-I	6th - 8th	Literature review, problem formulation, solution methodology, tools employed
5	Review-II	9th -10th	Analysis and implementation (partial)
6	Review-III	12th - 14th	Analysis, complete implementation and results.

Evaluation:

Evaluation of the project work carried out by each batch will be reviewed periodically by a review committee. Review committee consists of guide and two other faculty members who are guiding other batches. Generally, two to three reviews will be held during a semester. However, each project batch will be supervised by the guide on a weekly basis. Review committee will evaluate for 40% and guide will evaluate for 60% of the total marks.

Continuous Internal Evaluation (50%)	**Assessment**	**Weightage in Marks**
	Evaluation by Project Guide	30
	Project Review committee	20
Semester End Examination (50%)	Using SEE Rubrics	50
	Total	**100**

Passing: 40% both in CIE and SEE

Course Code: 17EEEC307 **Course Title: Automotive Electronics**
L-T-P-SS: 3-0-0 Credits:3 **Contact Hrs: 3 hrs/week**
CIE Marks: 50 SEE Marks: 50 **Total Marks: 100**
Teaching Hrs: 40hrs **Exam Duration: 3 hrs**

Unit I		
No	**Content**	**Hrs**
1	**Automotive Systems, Design cycle and Automotive industry overview** Overview of Automotive industry, Vehicle functional domains and their requirements, automotive supply chain, global challenges. Role of technology in Automotive Electronics and interdisciplinary design. Introduction to modern automotive systems and need for electronics in automobiles and application areas of electronic systems in modern automobiles, Introduction to power train, Automotive transmissions system ,Vehicle braking fundamentals, Steering Control, Overview of Hybrid Vehicles **ECU Design Cycle :** Types of model development cycles(V and A) , Components of ECU, Examples of ECU on Chassis, Infotainment, Body Electronics and cluster	**8**
2	**Automotive Sensors and Actuators:** Sensor characteristics, Sensor response, Sensor error, Redundancy of sensors in ECUs, Avoiding redundancy, Smart Nodes , Examples of sensors : Accelerometer (knock sensors),wheel speed sensors, Engine speed sensor, Vehicle speed sensor, Throttle position sensor, Temperature sensor, Mass air flow (MAF) rate sensor, Exhaust gas oxygen concentration sensor, Throttle plate angular position sensor, Crankshaft angular position/RPM sensor, Manifold Absolute Pressure (MAP) sensor. **Actuators**: Engine Control Actuators, Solenoid actuator, Exhaust Gas Recirculation Actuator.	**7**
	Unit II	
3	**Embedded system in Automotive Applications & Automotive safety systems:** Review of microprocessor, microcontroller and digital signal processor within the automotive context. Criteria to choose the right microcontroller/processor for various automotive applications, Architectural attributes relevant to automotive applications Automotive grade processors ex: Renesas, Quorivva, Infineon. **EMS:** Engine control functions, Fuel control, Electronic systems in Engines , Development of control algorithm for EMS, Look-up tables and maps, Need of maps, Procedure to generate maps, Fuel maps/tables, Ignition maps/tables, Engine calibration, Torque table, Dynamometer testing **Safety Systems in Automobiles: Active and Passive safety systems:** ABS, TCS, ESP, Brake assist, Airbag systems etc.	**10**
4	**Automotive communication protocols :** Overview of Automotive communication protocols : CAN, LIN , Flex Ray, MOST	**5**
	Unit – III	
5	**Advanced Driver Assistance Systems (ADAS) and Functional safety standards:** Advanced Driver Assistance Systems (ADAS):Examples of assistance applications: Lane Departure Warning, Collision Warning, Automatic Cruise Control, Pedestrian Protection, Headlights Control, Connected Cars technology and trends towards Autonomous vehicles. **Functional Safety:** Need for safety standard-ISO 26262, safety concept, safety process for product life cycle, safety by design, validation	**5**

6	**Diagnostics:** Fundamentals of Diagnostics: Basic wiring system and Multiplex wiring system, Preliminary checks and adjustments, Self-diagnostic system. Fault finding and corrective measures, Electronic transmission checks and Diagnosis, Diagnostic procedures and sequence, On board and off board diagnostics in Automobiles, OBDII, Concept of DTCs, DLC, MIL, Freeze Frames, History memory, Diagnostic tools, Diagnostic protocols : KWP2000 and UDS	**5**

Text Book:

1. Ribbens – Understanding of Automotive electronics
2. Denton.T – Automobile Electrical and Electronic Systems.
3. Denton.T – Advanced automotive fault diagnosis

References:

1. Ronald K Jurgen: "Automotive Electronics Handbook, 2nd Edition, McGraw-Hill, 1999
2. James D Halderman: -Automotive electricity and Electronics", PHI Publication
3. Terence Rybak. Mark Stefika: Automotive Electromagnetic Compatibility (EMC), Springer. 2004
4. Allan Bonnick.: "Automotive Computer Controlled Systems" Diagnostic Tools and Techniques". Elsevier Science, 2001
5. William T.M – Automotive Electronic Systems.
6. Nicholas Navet – Automotive Embedded System Handbook 2009.
7. BOSCH Automotive Handbook, 6th Edition.

Course Code: 19EEEC303 **Course Title: Object Oriented Programming using C++**

L-T-P: 2-0-1 Credits: 3 Contact Hrs: 3

ISA Marks: 50 ESA Marks: 50 Total Marks: 100

Teaching Hrs: 40 Exam Duration: 03 hrs

Content	Hrs
Unit - 1	
Chapter 01: Introduction Principles of Object Oriented Programming, Procedure oriented and Object oriented Programming, Basic Concepts of OOP, Benefits and Applications of OOP, Beginning with C++, Simple C++ program, C++ with classes, Structure of C++ program, Creating, compiling and linking C++ programs.	4 hrs
Chapter 02: Classes and Objects Structures and Classes, Specifying a Class, Defining Member functions, C++ program with class, Access Specifiers, Scope Resolution Operators, Inline functions, Static Data Members, Static Member Functions, Friend Functions.	7 hrs
Chapter 03: Constructors and Destructors Introduction, Parameterized Constructors, Multiple Constructors, Copy Constructor, Dynamic Constructor, Destructors, Dynamic allocation of objects - new and delete operators.	4 hrs
Unit - 2	
Chapter 04: Inheritance Introduction, Defining Derived Classes, Types of Inheritance, Virtual Base Classes, Abstract Classes, Constructors in Derived Classes, Nesting of Classes.	6 hrs
Chapter 05: Virtual Functions and Polymorphism Pointers to objects, this pointer, Pointers to Derived classes, Virtual Functions. Pure Virtual Functions.	5 hrs
Chapter 06: Exception Handling Basics, Exception Handling Mechanism, Throwing, Catching and Rethrowing Exceptions.	4 hrs
Unit - 3	
Chapter 07: Function Overloading, Operator Overloading Function Overloading, Overloading Constructors, Defining operator Overloading, Unary and Binary operator overloading, Rules for overloading operators.	5 hrs
Chapter 08: Templates, STL Class Templates, Function Templates, Overloading of Template functions, Components of STL, Containers, Iterators, Application of Container Classes.	5 hrs

Text Books (List of books as mentioned in the approved syllabus)

1. E.Balagurusamy, Object Oriented Programming with C++, 4th edition, Tata McGrawHill, 2008
2. Herbert Schildt, C++ The Complete Reference, Fourth Edition, Tata McGrawHill, 2003

References

1. Yashavant P. Kanetkar, Let Us C++, 1st, BPB Publications,
2. Stanley B.Lippmann, Josee Lajore, Barbara E. Moo, C++ Primer, 4th Edition, Pearson Education, 2005

Course Code: 19EEEE301	Course Title: CMOS VLSI Circuits	
L-T-P: 3-0-0	Credits: 3	Contact Hrs: 40
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3 hrs

Content	Hrs
Unit – 1	
Chapter No. 1. Introduction to VLSI and IC fabrication technology VLSI Design Flow, Semiconductor Technology - An Overview, Czochralski method of growing Silicon, Introduction to Unit Processes (Oxidation, Diffusion, Deposition, Ion-implantation), Basic CMOS technology - Silicon gate process, n-Well process, p-Well process, Twin-tub Process, Oxide isolation.	06 hrs
Chapter No. 2. Electronic Analysis of CMOS logic gates DC transfer characteristics of CMOS inverter, Beta Ratio Effects, Noise Margin, MOS capacitance models. Transient Analysis of CMOS Inverter, NAND, NOR and Complex Logic Gates, Gate Design for Transient Performance, Switch-level RC Delay Models, Delay Estimation, Elmore Delay Model, Power Dissipation of CMOS Inverter, Transmission Gates & Pass Transistors, Tristate Inverter.	14 hrs
Unit – 2	
Chapter No. 3. Design of CMOS logic gates Stick Diagrams, Euler Path, Layout design rules, DRC, Circuit extraction, Latch up – Triggering Prevention.	06 hrs
Chapter No. 4. Designing Combinational Logic Networks Gate Delays, Pseudo nMOS, Clocked CMOS, Dynamic CMOS Logic Circuits, Dual-rail Logic Networks: CVSL, CPL.	08 hrs
Unit – 3	
Chapter No. 5. VLSI Design Flow Structured Design Strategies: Hierarchy, Regularity, Modularity, Locality, SDEF Layout Flow, Case Study IC tape out.	06 hrs

Text Books (List of books as mentioned in the approved syllabus)

1. John P. Uyemura, Introduction to VLSI Circuits and Systems, 1, Wiley, 2007
2. Neil Weste, David Harris & Ayan Banerjee, CMOS VLSI Design, 3, Pearson Ed, 2005
3. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3, Tata McGra, 2007

References

1. Wayne, Wolf, Modern VLSI design: System on Silicon, 3, Pearson Ed, 2005
2. Douglas A Pucknell and Kamran Eshraghian, Basic VLSI Design, 3, PHI, 2005
3. Phillip. E. Allen, Douglas R. Holberg, CMOS Analog circuit Design, 1, Oxford University, 2002

Course Code: 19EEEE302	Course Title: **Battery Management Systems**	
L-T-P: 3-0-0	Credits: 3	Contact Hrs: 40
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3 hrs

Content	Hrs
Unit - 1	
Chapter No. 1. Introduction: Introduction to electric vehicle & hybrid electric vehicle, types of batteries and their specific applications, Lithium-ion battery fundamentals: Battery Operation, Battery Construction, Battery Chemistry, Safety, Longevity, Performance, and Integration. (introduction to broad spectrum of batteries)	03 hrs
Chapter No. 2. Battery Models: Battery Models, Overview, self-Discharge Modeling and parameter identification using SOC/OCV , Thevenin Equivalent Circuit, Hysteresis, Coulombic Efficiency, Nonlinear Elements	4 hrs
Chapter No. 3. BMS (Black-box approach): Need for BMS, Typical inputs, typical outputs and typical functions Battery management system network in a typical electric vehicle	2 hrs
Chapter No. 4. BMS Architectures: Monolithic, Distributed, Semi-Distributed, Connection Methods, Additional Scalability, Battery Pack Architectures	2 hrs
Chapter No. 5. System Control: Contactor Control, Soft Start or Precharge Circuits, Control Topologies, Contactor Opening Transients, Chatter Detection, Economizers, Contactor Topologies, Contactor Fault Detection	4 hrs
Unit - 2	
Chapter No. 6. Data acquisition (Measurement): Cell voltage, current and temperature measurement, Synchronization of Current and Voltage **(5 hrs)**	5 hrs
Chapter No. 7. Battery Management System Functionalities: CC/CV Charging Method, Target Voltage Method, Constant Current Method, Thermal Management, and Operational Modes.	3 hrs
Chapter No. 8. Charge Balancing(Cell balancing): Charge Balancing Strategies, Balancing Optimization, Charge Transfer Balancing, Flying capacitor	5 hrs
Chapter No. 9. SoC Estimation: Columb counting, SoC corrections, OCV measurements, temperature compensation	2 hrs
Unit - 3	
Chapter No. 10. BMS communications: Overview, Network Technologies ,I2C/SPI, RS-232 and RS-485 134, Local Interconnect Network, CAN 136 ,Ethernet and TCP/IP ,Modbus ,FlexRay, Network Design	5 hrs
Chapter No. 11. Battery Safety: Functional Safety, Hazard Analysis, Safety Goals, Safety Concepts and Strategies, Reference Design for Safety.	5 hrs

Text Books

1. Phillip Weicker*"A Systems Approach to Lithium-Ion Battery Management"* 2013, Artech house publisher

References

1. Jiuchun Jiang and Caiping Zhang, "*Fundamentals and Applications of Lithium-Ion Batteries in Electric Drive Vehicles*", John Wiley & Sons, 2015

Course Title: Power Electronics & Drives Lab		Course Code: 20EEEP301
L-T-P: 0-0-1	Credit:1	Contact Hours: 2hrs/week
CIE Marks:80	SEE Marks: 20	Total Marks:100
Laboratory Hours: 2hrs	Exam Duration:2 hrs	

Expt. No.	List of Experiments
	Demonstration
1.	Introduction to Sciamble workbench software
2.	Generation of PWM pulses
3.	Rapid Control Prototyping (RCP) using Model Based Design software
	Exercise
1.	Characterization of a DC motor.
2.	DC motor speed control
3.	Four Quadrant Operation of the DC Motor
4.	Volts/Hertz control of three-phase induction motor.
	Structured Enquiry
1.	To design and mathematically model the DC/IM drive. Experimentally verify the operability of the controller design using workbench.

Laboratory Title: Automotive Electronics Lab **Lab. Code: 17EEEP305**
Total Hours: 36 Hrs **Duration of Exam: 03 Hrs**
Total Exam Marks: 100 **Total CIE. Marks: 80**

Sl. No.	Name of Experiment
	Demonstration Experiment
1	Electronic engine control system: Injection and Ignition control system, Transmission trainer modules
	Exercise Experiment
2	Simulation of an automobile engine
3	Modeling a vehicle motion on a flat surface during hard acceleration, deceleration and steady acceleration.(ABS and suspension system)
4	Basic gate logic simulation and modeling using Simulink and realization on the hardware platform.
5	Modeling Seat belt warning system, and Vehicle speed control based on the gear input.
6	EGAS modeling and simulation using Simulink and realization on the hardware platform.
7	Interior lighting control modeling with state flow
8	Gear input transmission over CAN bus using ARM Cortex m3 and signal analysis using CANalyzer/BusMaster software. Code driven and Model driven integration for Vehicle speed control function based on the gear input.
	Structured Enquiry
1	Develop Matlab code for stepper motor control and convert it to Simulink model and port it on to an embedded hardware
2	Develop a C code for LCD display device and convert it to Simulink model and port it to embedded hardware/FPGA

Laboratory Title: Minor Project **Lab. Code: 17EEEW302**

Total Hours: 36 **Duration of SEE Hours: 3**

SEE Marks: 50 **CIE Marks: 50**

Students are supposed to carry out the minor project based on the theme and guidelines as given below.

(I) Theme:

Hardware Design and Implementation of Electrical and / or Electronics System for application in Controls, Measurement and Instrumentation, Power Electronics and Drives, Relays, Renewable Energy Systems etc using specialized ICs /Microcontrollers /DSPs.

(II) Project batches and Guide:

Each project batch consists of 3 or 4 students. Students are informed to form their own batch based on the kind of project work and their interest. Each batch is supposed to give four faculty names as guides in the order of their preference. Guides will be allocated based on the preference given by the batch. The primary role of the guide is to supervise the work, provide appropriate guidance in successfully carrying out the project work.

(III) Project implementation

The principle steps in carrying out the project work are summarized below:

Step-1: Literature survey:

A literature survey with regard to the given theme is to be carried out in order to understand the state of the current research. Further, a critical review of the collected literature will facilitate to summarize key observations. Key observations will lead to identifying a specific problem for the project work in terms of alternate/new solution techniques, possible improvements, new formulations or models, hardware implementations etc.

Step-2: Prepare a synopsis:

A synopsis highlights the definition of identified problem and its significance. The synopsis will also contain detailed literature review giving the state of the current research on the selected specialized area. It will also brief the problem formulation, solution methodology, tools employed and possible outcomes.

Step-3: Project implementation:

The work is to be carried out in phase wise manner, testing or analyzing the partial results obtained. Guide will periodically monitor the progress of the work done giving suitable suggestions as required.

(IV) Schedule:

Sl. No.	Activity	Week No.	Evaluation Objectives
1	Announcement for the formation of batches	At the end of the previous semester	NA
2	Allotment of guides	1st - 2nd	NA
3	Submission of Synopsis	3rd - 5th	Literature review, problem formulation, solution methodology, tools employed
4	Review-I	6th - 8th	Literature review, problem formulation, solution methodology, tools employed
5	Review-II	9th -10th	Analysis and implementation (partial)
6	Review-III	12th - 14th	Analysis, complete implementation and results.

Evaluation:

Evaluation of the project work carried out by each batch will be reviewed periodically by a review committee. Review committee consists of guide and two other faculty members who are guiding other batches. Generally, two to three reviews will be held during a semester. However, each project batch will be supervised by the guide on a weekly basis. Review committee will evaluate for 40% and guide will evaluate for 60% of the total marks.

Continuous Internal Evaluation (50%)	Assessment	Marks
	Evaluation by Project Guide	30
	Project Review committee	20
Semester End Examination (50%)	Using SEE Rubrics	50
	Total	**100**

Passing: 40% both in CIE and SEE

Course Code:17EEEC401 **Course Title: Switched Mode Power Converters**

L-T-P-SS: 3-0-0 Credits: 3 Contact Hrs: 40

CIE Marks: 50 SEE Marks: 50 Total Marks: 100

Teaching Hrs: 40 Exam Duration: 3 hrs

Chapter No.	Unit-I	
1	**Chapter No. 1.DC Power Supplies:** Introduction, transformer models, the flyback converter: Continuous Current Mode, Discontinuous Current Mode, Summary of flyback converter operation, the forward converter, summary of forward converter, operation, the doubly ended (two switch)forward converter, the push-pull converter, summary of push-pull converter operation, full-bridge and half-bridge DC-DC converters, multiple outputs, converter selection, power factor correction, simulation of DC power supplies, pwm control circuits, the Ac line filter, the complete DC power supply .	15 hrs
	Unit-II	
2	**Chapter No. 2. DC-AC Switched Mode Inverters** Introduction, basic concepts of switch-mode inverters, single phase inverters, three phase inverters, effect of blanking time on output voltage in inverters, other inverter switching schemes, rectifier mode of operation.	15 hrs
	Unit-III	
3	**Chapter No. 3. Multilevel Converters:** Introduction, Generalized topology with a Common DC Bus, Converters Derived from the Generalized Topology, Diode Clamped Topology, Flying Capacitor Topology,	05 hrs
4	**Diode Clamped Multilevel Converters:** Introduction, Converters structure and Functional description: voltage clamping, switching logic, Modulation of multilevel converters, Multilevel space vector modulation	05 hrs

Text Books

1 Ned Mohan, T. M. Undeland and W. Robbins, Power Electronics: Converters, Applications and Design, 2, John Wiley and Sons, 1995

2 Daniel W Hart, Power Electronics, 1, Tata McGRAW-HILL, 2011

3 YorkSergio Alberto González, Santiago Andrés Verne, María Inés Valla, Multilevel converters for Industrial Applications, CRC Press, 2014 .

Reference Books:

1 Rashid M. H, Power Electronics: Circuits, Devices and Applications, 3, PHI, 2005

2 Bose B. K., , Power Electronics and AC Drives, 5, PHI, 2003

3 Rashid M. H, Digital Power Electronics and Applications, 1, Elsevier, 2005

4 V. Ramanarayanan, Switched Mode Power Converters Notes, IISC, Bangalore, 2008

Course Code: 21EEEE402	Course Title: AUTOSAR	
L-T-P : 3-0-0-0	Credits: 3	Contact Hrs: 3 Hours
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3

Content	Hrs
Unit - 1	
Chapter No. 1: AUTOSAR Fundamentals Evolution of AUTOSAR – Motivations and Objectives AUTOSAR consortium – Stake holders – work Packages, AUTOSAR Partnership, Goals of the partnership, Organization of the partnership, AUTOSAR specification, AUTOSAR Current development status, BSW Conformance classes: ICC1, ICC2, ICC3, and Drawbacks of AUTOSAR.	8 hrs
Chapter No. 2: AUTOSAR layered Architecture AUTOSAR Basic software, Details on the various layers , Details on the stacks Virtual Function Bus (VFB) Concept Overview of AUTOSAR Methodology , Tools and Technologies for AUTOSAR AUTOSAR Application Software Component (SW-C) ,Types of SW-components AUTOSAR Run Time Environment (RTE): RTE Generation Process: Contract Phase, Generation Phase, MCAL, IO HW Abstraction Layer, Partial Networking, Multicore, J1939 Overview, AUTOSAR Ethernet, AUTOSAR E2E Overview , AUTOSAR XCP, Metamodel , From the model to the process , Software development process.	7 hrs
Unit - 2	
Chapter No. 3: Methodology of AUTOSAR and Communication in AUTOSAR CAN Communication, CAN FD, CANape, Application Layer and RTE, intra and inter ECU communication, Client-Server Communication, Sender-Receiver, Communication, CAN Driver, Communication Manager (ComM), Overview of Diagnostics Event and Communication Manager	10 hrs
Chapter No. 4: Overview about BSW constituents BSW Constituents: Memory layer, COM and Services layer, ECU abstraction, AUTOSAR, Operating system, Interfaces: Standard interface, AUTOSAR standardized interface, BSW-RTE interface,(AUTOSAR interface), BSW-ECU hardware interface, Complex device drivers and BSW module configuration, AUTOSAR Integration.	5 hrs
Unit - 3	
Chapter 5: MCAL and ECU abstraction Layer Microcontroller Drivers, Memory drivers: on-chip and off chip drivers, IO drivers(ADC, PWM, DIO), Communication drivers: CAN driver, LIN drivers, Flexrfay	5 hrs
Chapter 6: Service Layer Diagnostic Event Manager, Function inhibits Manager, Diagnostic communication manager, Network management, Protocol data unit router, Diagnostic log and trace unit, COMM manager.	5 hrs

Text Book (List of books as mentioned in the approved syllabus)

1. Ribbens, Understanding of Automotive electronics, 6th Edition, Elsevier, 2003
2. Denton.T, Automobile Electrical and Electronic Systems, Elsevier, 3rd Edition, 2004
3. Denton.T, Advanced automotive fault diagnosis, 2000

References

1. Ronald K Jurgen, Automotive Electronics Handbook, 2nd Edition, McGraw-Hill, 1999
2. James D Halderman, Automotive electricity and Electronics, PHI Publication, 2000
3. Allan Bonnick, Automotive Computer Controlled Systems Diagnostic Tools and Techniques, Elsevier Science, 2001
4. Nicholas Navet , Automotive Embedded System Handbook , 2009

Course Title: Powertrain Control Laboratory		Course Code: 20EEEE402
L-T-P: 0-0-3	Credit:3	Contact Hours: 2hrs/week
CIE Marks:80	SEE Marks: 20	Total Marks:100
Laboratory Hours: 2hrs	Exam Duration:2 hrs	

Expt. No.	List of Experiments
	Demonstration
1.	Introduction to MATLAB Simulink
	Exercise
1.	Battery Modelling and simulation
2.	Mathematical modelling and simulation of power converters
3.	dq transformation theory
4.	Characterization of a three phase induction motor
5.	Induction motor drive
6.	PMSM Drive
7.	PMBLDC Drive
	Structured Enquiry
1.	System Integration and testing (End-to-end simulation)

Course Code: **17EEEE405**	Course Title: **Smart Grid Technologies**	
L-T-P-SS: 3-0-0-0	Credits: 3	Contact Hrs: 40
CIE Marks: 50	SEE Marks: 0	Total Marks: 50
Teaching Hrs: 40		Exam Duration: 3 hrs

Chapter No.	**Unit-I**	
1	**Chapter No. 1. Introduction to energy efficient smart grids** Concept, Defining a perfect electric energy service system, Fully integrated power systems: Smart grids, Challenges in Smart grids implementation**:** Enabling Energy Efficiency, Overview of the technologies required for energy efficient smart grids.	4 hrs
2	**Chapter No. 2. Communication technology in smart grids** Communication requirements, Overview of smart grid standards, Wired and wireless Communication, Communication Networks: Wide area network, Neighborhood area networks, home are networks, Integration of Utility Communication Networks and Smart Devices, Cyber security, Interoperability, Case Studies	8 hrs
	Unit II	
3	**Chapter No. 3. Smart and Efficient Transmission System** Transmission Blackouts: Risk, Causes and Mitigation and Case Studies, Phasor measurement unit, Phasor data concentrators, Wide Area Monitoring, Protection and Control, Energy Monitoring systems and its applications in Smart grids, Flexible AC and HVDC transmission system.	7 hrs
4	**Chapter No. 4. Protocols and Standards in Smart systems** International Electro-technical communication standards and benefits, BEE standards for Implementation of Energy Management System, GOOSE protocols for communication, IEC 61850 Substation model, Integration of Intelligent Electronic Devices in EMS, SCADA and Substation Automation Systems.	7 hrs
	Unit III	
5	**Chapter No. 5. Smart Distribution systems and Energy Storage** Smart metering, Real time energy pricing, Smart appliances, Distributed Energy Resources in Smart Grids, Demand response, Energy Storage Devices: Battery storage, Plug in hybrid electric vehicles, Compressed air, Pumped hydro, Ultra capacitors, Fly wheels and Fuel cells	7 hrs
6	**Chapter No. 6. Renewable Energy integration** Carbon foot printing, Micro-grid architecture, Modeling PV and Wind systems, Tackling Intermittency, Issues of interconnection, Protection and control of Micro-grid and sustainability	7 hrs

Text Books	
1	Janaka Ekanayake, Nick Jenkins, Kithsiri Liyanage Jianzhong, Wu Akihiko Yokoyama, Smart Grid : Technology and Applications, 1st edition March 2012, Wiley.
2	Clark .W Gellings, The Smart Grid : Enabling Energy Efficiency and Demand Response, Published by The Fairmont Press, CRC Press by Taylor and Francis Group, LLC
Reference Books:	
1	Stuart Borlase, Smart Grids(Power Engineerirng), 1, CRC press, 2012
2	Joao P.S. Catalao, Smart Grids and Sustainable Power Systems, CRC press, 2015 by Taylor and Francis Group, LLC
3	Bureau of Energy Efficiency: Standard Guide Books for Energy Auditors and Managers, Ministry of power, Govt. of Bhaarat.

Course Code: 19EEEE401 L-T-P**: 3- 0- 0**
Course Title: **Flexible AC Transmission System (FACTS)** CIE Marks: **50**
Teaching Hrs: **40 hrs** SEE Marks: **50**

	UNIT I	Hrs
1.	**FACTS: Concept and General System Considerations:** Transmission Interconnection, Flow of power in AC system, Limits of loading capability, Power flow and dynamic stability consideration of a Transmission Interconnection, Relative importance of controllable parameters, and Basic types of FACTS controllers, Brief description and Definitions of FACTS controllers, Perspective: HVDC or FACTS	10 hrs
2.	**Voltage Sourced Converters:** Basic Concepts, Single Phase Full Wave Bridge Converter Operation, Single phase Leg operation, Three Phase Full Wave Bridge Converter, Transformer Connection for 12 pulse operation	05 hrs
	UNIT II	
3.	**Current Sourced Converters:** Basic concepts, Three phase full wave diode rectifier, Thyristor based converter Rectifier operation with gate turn ON, Current sourced converter with turn OFF devices, Current sourced versus Voltage sourced converter.	05 hrs
4.	**Objectives of Series and Shunt Compensation:** Objective of Shunt Compensation, Methods of Controllable VAR Generation, Static VAR Compensators SVC STATCOM, Objective of Series Compensation, Static Series Compensators, GCSC, TSSC, TCSC and SSSC	10 hrs
	Unit – III	
5.	**Static Voltage, Phase Angle Regulators:** Objectives of Static Voltage and Phase Angle Regulators, Approach to Thyristor Controlled Voltage and Phase Angle Regulators, TCVR and TCPAR,	05hrs
6.	**Combined Compensators:** Unified Power Flow Controller UPFC and Interline Power Flow Controller IPFC.	05hrs

Text Book:

1. Narain G. Hingorani, and Laszlo Gyugyi., "*Understanding FACTS*", IEEE Press, Standard Publishers Distributors, Delhi, 200, ISBN 81 86308 79 2.

References Book:

1. K. R Padiyar, "*FACTS controllers in Power Transmission and Distribution",* New Age International Publishers, New-Delhi, 2007, ISBN 978 81 224 2142 2.

Laboratory Title: Power System Simulation Lab **Lab. Code: 19EEEP401**

Credits: L-T-P: 0-0-1 **Credits: 1** **Duration of SEE Hours: 2**

SEE Marks: 20 **CIE Marks: 80**

Experiment wise Plan

List of experiments/jobs planned to meet the requirements of the course.

Category: Demonstration	
Expt./ Job No.	Experiment / Job Details
1	To use interactive simulation software "SofTCAPS" for the simulation of (i)Load flow analysis by Gauss-Seidel and NR models (ii) Voltage control analysis by shunt capacitor and tap changing transformer (iii) P-V Curve at a load bus
2	To use interactive software "SofTCAPS" for the simulation of Economic load dispatch problem with and without coordinating the transmission losses
Category: Exercise	
Expt./ Job No.	Experiment / Job Details
3	To form bus admittance matrix [Ybus] by singular transformation.
4	To form [Ybus] by the method of inspection
5	ABCD constants and line performance using short and medium π/T models
Category: Structured Enquiry	
Expt./ Job No.	Experiment / Job Details
6	Each batch (consisting of 4 students) will work on one problem from the below mentioned sets, obtain the simulation results, carry out the analysis, interpret the results, draw practical conclusions from them and prepare a report. (a) To formulate and develop MATLAB/Scilab program/ SIMULINK model on one of the power problem which include, but not limited to - Load frequency control method, Study to determine the effect of excitation on dynamic stability, Comparison of various numerical techniques for stability study, Multimachine transient stability study, Load flow model development, (b) To employ an interactive power system software to simulate a given problem such as multimachine transient stability, multimachine small signal stability, contingency analysis, performance comparison of various load flow models, economic load dispatch etc.

KLE Technological University (Creating Value, Leveraging Knowledge)	FORM ISO 9001: 2008 – BVBCET	Document #: FMCD2005	Rev: 1.0
Department of Electrical & Electronics Engineering			

Laboratory Title: **Relay & High Voltage Lab**		Lab. Code: 20EEEP401
Total Hours: **32**	Credits: L-T-P**: 0-0-2** Credits: 2	Duration of SEE Hours: 2
SEE Marks: **20**		CIE Marks: **80**

Expt./ Job No.	**Experiment / Job Details**	
Category: Exercise		
1	Introduction Session	2 hrs
2	To obtain the inverse time characteristics of a given fuse wire and wires of different lengths.	2hrs
3	To obtain the inverse time characteristics of an electromagnetic over current relay	2hrs
4	To obtain the operating characteristics of microprocessor based differential relay.	2hrs
5	To obtain the operating characteristics of microprocessor based directional over current relay.	2hrs
6	To obtain the breakdown strength of air using Copper sphere gap with HVAC and HVDC.	2hrs
7	a) To obtain the breakdown strength of air using different pairs of electrode gap with HVAC and HVDC. b) To obtain the breakdown voltage of a solid dielectric. c) To obtain the breakdown voltage of a liquid dielectric.	2hrs
Category: Structured Enquiry		
1.	To develop microcontroller based overcurrent, over voltage and impedance relay using CT /PT giving details of program and demonstrate it's working output.	4hrs

Laboratory Title: **Senior Design Project**	Lab. Code: 21EEEW401
Total Hours: **50**	Duration of ESA Hours: 3
ESA Marks: **50**	ISA Marks: **50**

Senior Design Project Guidelines

(I) Preamble

A project work essentially gives the students a platform to integrate the concepts studied during the study, enhance their analytical capabilities and develop abilities to effectively communicate technical information in multiple formats. During the course of projects, students are asked to follow the research methodology in identifying a problem of their interest though literature survey, carry-out feasibility study, formulate the problem, develop mathematical models, select suitable solution technique etc. Students are also encouraged to develop new formulations, alternate solution techniques, study and apply new optimization algorithms, develop new simulation models and use modern engineering/simulation tools.

(II) Project batch and Guide

Each project batch consists of 3 or 4 students. Students will be informed to form their own batch based on the kind of project work and their interest. Each batch is supposed to give four faculty names as guides based on faculty expertise in the order of their preference. Guides will be allocated based on the preference given by the batch. The primary role of the guide is to supervise the work, give appropriate guidance in successfully carrying out the project work.

(III) Project implementation

The principal steps in carrying out the project work are summarized below:

Step-1: Selection of a specialized area for the project work

A specialized area in which the project work is to be carried out depends on the interest and specialized skills acquired by the project team. This includes areas such as power system analysis, power system dynamics, renewable energy, electric drives, VLSI & Embedded system, Power quality issues etc. The proposed work may include simulation studies, hardware implementation or both.

Step-2: Selection of topic based on literature survey

A literature survey in the selected specialized area is to be carried out in order to understand the state of the current research. Further, a critical review of the collected literature will facilitate to summarize key observations. Key observations will lead to identifying a specific problem for the project work in terms of alternate/new solution techniques, possible improvements, new formulations or models, hardware implementations etc.

Step-3: Prepare a synopsis

A synopsis highlights the definition of identified problem and its significance. The synopsis will also contain detailed literature review giving the state of the current research on the selected specialized area. It will also brief the problem formulation, solution methodology, tools employed and possible outcomes.

Step-4: Project implementation

The work is to be carried out in phase wise manner, testing or analyzing the partial results obtained. Guide will periodically monitor the progress of the work done giving suitable suggestions as required.

(IV) Schedule

Sl. No.	Activity	Week No.	Evaluation Objectives
1	Announcement to form the batches	At the end of the previous 7th sem	NA
2	Allotment of guides	1st- 2nd	NA
3	Submission of Synopsis	4th- 5th	Literature review, problem formulation, methodology by respective Guides
4	Review-I	6th - 8th	Literature review, problem formulation, methodology, tools used in the presence Review Committee
5	Review-II	9th -10th	Implementation and analysis done
6	Review-III	12th - 14th	Completion along with Hardware/ Software/ Report. Results and Conclusions.

(V) Evaluation

Evaluation of the project work carried out by each batch will be reviewed periodically by a review committee. Review committee consists of guide and two/ three other faculty members who are guiding other batches. Generally, two to three reviews will be held during a semester. However, each project batch will be supervised by the guide on a weekly basis. Review committee will evaluate for 40% and guide will evaluate for 60% of the total marks.

Activity	Assessment	Marks
ISA (50%)	Project Review committee	30
	Evaluation by Project Guide	20
ESA (50%)	Using ESA Rubrics	50
	Total	**100**

Passing: 40% both in ISA and ESA

Course Title: Research Experience for undergraduates	Course Code: 17EEEE490
L-T-P: 0-0-6	Duration of ESA: 1hr
ESA Marks: 50	CIE Marks: 50

REU courses

Course on Research Methodology (RM)

Sl no.	Topic	Time
1	Overview of course on research methodologies	2 hrs (First week)
1	How to carry out literature review	3 hrs (First week)
2	Problem definition/formulation Data Interpretation	2 hrs (First week)
3	Research Design	2 hrs (First week)
4	Report writing	1hrs (Mid of summer sem)
5	Paper writing	1hrs (Mid of summer sem)

Details of Phases of REU Courses

Sl No.	Phases	Reviews	Items to be reviewed	Outcome Elements	Max Marks	CLO	BL
1	Phase-1 During summer semester	Review-1 Before the end of 2 week	Idea-Generation: Literature survey, (familiarity of the problem), different solutions, Tool learning, expt setup, requirement analysis and RoadMap	1.1.4, 2.1.2, 2.4.1, 3.1.3, 4.1.1, 4.2.1, 4.3.1, 5.2.1, 5.3.1, 6.1.1, 6.2.2, 8.2.2, 10.1.1, 12.3.1	25	1,2	4,5
		Review-2 Before the end of 6 week	Procedures/Design Phase Implementation - p1	2.1.2, 2.4.1, 3.1.3, 4.1.1, 4.2.1, 4.3.1, 5.2.1, 5.3.1,	25	3,4	4,5

				6.1.1, 6.2.2, 8.2.2, 10.1.1, 11.1.1 13.1.1			
		Review-3 End of the semester	Implementation -p2 continuation with the course	2.1.2, 2.4.1, 3.1.3, 4.1.1, 4.2.1, 4.3.1, 5.2.1, 5.3.1, 6.1.1, 6.2.2, 8.2.2, 10.1.1, 11.1.1 13.1.1	25	3,4,5	4,5,6
2	Phase-2 During odd semester	Review-4	Demonstration of results, report writing, presentation, paper writing	1.1.4, 2.1.2, 2.4.1, 4.1.1, 4.2.1, 4.3.1, 5.2.1, 5.3.1, 9.1.1, 10.1.1, 12.3.1 14.1.1 14.1.2	25	3,4,5,6	4,5,6
3	Phase-3 End of the odd semester	Viva-voce At the beginning of 8th semester	Viva-voce with the external examiner		100		

Evaluation Rubrics

Name of the student:

Name of the guide/s:

Name of the committee members:

Note:

1. For the final grading total marks are normalized to 100: 50% (50 from 100) marks from the CIE and 50% (50 from 100) marks from SEE shall contribute.
2. 20% of CIE (20 marks from 100) are from course on research methodology.
3. Review committee shall be appointed by DUGC with HOD/HOS as chairman.

4. Use the REU style file already given to the students
5. Evaluate the contribution as weak (W), moderate (M) and strong (S).

Sl. no.	Reviews	Details		Contribution	Remarks
1	Course on RM (20)	3 Assignments			
Phase-1 Summer sem CIE-50M	Review -I (10 M), by guide	Problem Formulation	Literature survey		
			Identify gaps		
			Problem definition		
		Pre-requisits	Requirements		
			Demonstration of ability to use the tools/expt. setup		
			Planned activity chart		
	Review-II (10 M) by guide /s	Review of implementation-p1			
	Review-III (20 M) by committee	Committee review to decide continuation of the registration			
Phase-2 7th sem CIE-50M	Review-IV (20M) by guide/s	Review of implementation-p2			
	Review-V(20M) by committee	Demonstration of results, report writing, paper writing and presentation			
Phase-3 SEE	Dissertation (50 M) By guide/s	Citations,			
	Viva-voce(50 M) External +guide/s				
	Total: 200Marks				

Laboratory Title: Institutional Research Project (IRP)	Lab. Code: 21EEEE491
Total Hours: 75hrs	Duration of exam: **2 hours**
Total Exam Marks: **100**	ISA Marks: **50**

Guidelines for selection of a project:

- Researchers from the University apply for the research funding individually or in collaboration with national importance institutions to the agencies like DST, AICTE, VGST, DRDO, Agriculture Universities, industries. Faculty also apply for institutional funding to carry out research to provide an engineering solution for a societal problem.
- Once funding is confirmed, the Research and Development cell release Call For Participation (CFP) across the campus mentioning the details of all IRP/SRP/ISP.
  - Applications are scrutinized by the IRP/SRP/ISP team and an eligible team of students is allocated with the sub-module of the project.
  - Time plan: Research work worth of 60-70Hrs per team is assigned, including capacity building of individual members (80-100 Hrs) and teamwork (60-75hrs).

Criteria for group formation:

- 3-4 students in a team.
- Role of teammates: Team lead and members.

Allocation of Guides/ Mentors for the projects:

IRP/SRP/ISP faculty team will mentor the students' team

Role of a Guide/ Mentor

The primary responsibility of the mentor is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, a mentor should help towards its successful completion as per the predefined standards.

How student should carry out a project:

- Define the problem.
- Specify the requirements.
- Specify the design in an understandable form (Block Diagram, Flowchart,Algorithm, etc).
- Analyze the design and identify hardware and software components separately.
- Select appropriate simulation tool and development board for the design.
- Implement the design.
- Optimize the design and generate the results.
- Result representation and analysis.
- Prepare a document and presentation.

Report Writing

- The format for report writing should be downloaded from ftp://10.3.0.3/projects
- The report needs to be shown to guide and committee for each review.

Evaluation Scheme

- Internal semester assessment (ISA)
- Evaluation is done based on the evaluation parameters and rubrics given in Table 1, and Table 2 respectively.
- The progress of the project is reviewed and evaluated by the concerned team.

Table 1: Evaluation parameters for ISA

Reviews	Stages of projects	Parameters	Outcome Elements	Max Marks	Marks obtained
Review 1 (20M)	Initiation	Need analysis and Identification of problem	5.1.1	3	
		Problem relating socio economic context	7.1.2	3	
		Problem definition and application	6.1.1	3	
		Identifying multiple solutions, selecting the best suited solution and justifications with support of technical literature	10.1.1	5	
		Identify the standards and like IEEE& ACM Professional code of conduct	6.2.2 8.2.1	3	
		Identify limitations in the objectives and sources of error	2.4.3	3	
Review 2 (20M)	Planning	Project Planning (Gantt chart) and WBS(Work Breakdown Structure)	9.3.1	3	
		Identify the individual task	11.3.1	3	
		Mathematical and physical model of a system	2.3.2	3	
		Collection of appropriate test data	4.3.1	3	
		Functional block diagram relating input & output	5.2.2	3	
		Simulation of the design using suitable open source	5.2.1	3	
		Verify the credibility of results w.r.to accuracy and limitations	5.3.2	2	

Review 3 (40M)	Execution	Detailed block diagram with all hardware specifications	14.2.1	5	
		Detailed block diagram with all software specifications	14.2.2	5	
		Integrating the functional blocks, debugging details and partial demonstration of results	3.4.1	5	
		design and develop considering modern techniques under the constraints	14.2.2	5	
		Demonstrate the results	14.4.1	10	
		Plan for optimization	10.1.1	5	
		Draft copy of technical report	12.3.1	5	
Review 4 (20M)	Closure	Implementation, analysis and conclusion of the results (Pre optimization and post optimization discussion)	14.2.2	10	
		Report submission in Latex (as given in the format)	10.3.2	10	
		Budget for the project	11.3.2	7	
		Future improvement of the project	12.1.1	3	
		Deliver effective oral presentation	10.2.2	10	

Table 2: Evaluation Rubrics

Review	Sl. No	Description	Marks	Inadequate Up to 25%	Average Up to 50%	Admirable Up to 75%	Outstanding Up to 100%
R1	1.	Need Analysis and identifying the problem.	5	Not done	Not well defined	Framed but not clear	Need analysis done.
	2.	Understanding of professional ethics Copyright, plagiarism.	5	Does not understands	Understands and not considered	Understands and considered	Understands thoroughly and planned to address
	3.	Problem definition and Application in the societal context.	5	The problem definition is not stated correctly.	Aware of the problem but objectives and scope not well defined.	Overall sound understanding of the problem and constraints.	Problem and scope are well defined to the proposed work.
	4.	Identifying multiple solutions and selecting the	5	Not developed	Developed few (min 3) alternate solutions.	Developed alternate	Developed alternate solutions and selection of

		best-suited solution and justifications with support of technical literature.		alternate solution.		solutions but no evaluation.	optimal solutions.
R2	1	Project Planning (Gantt chart) and WBS(Work Breakdown Structure).	5	Work distribution is not done.	The leader identified, but work is not started	The leader identified, but work is not distributed properly.	The leader identified, and work has been distributed properly.
	2	Specification and identification of input & output.	5	Input and output are not identified.	Input and output are identified.	Input and output are identified but not according to specs.	Inputs, outputs are identified and are according to specs
	3	Functional block diagram relating. input & output	5	Incomplete functional block diagram	The functional block diagram is done but inputs outputs are not stated.	The functional block diagram is done but inputs and outputs are not clearly mentioned.	The functional block diagram is done with proper inputs and outputs are not clearly mentioned.
	4	Simulation of the design using any open source.	5	No results and no analysis	Partial results but no analysis.	Inadequate analysis	Desired results are obtained and analyzed.
R3	1	Detailed block diagram with all specifications/ algorithms	5	Incomplete block diagram	The functional block diagram is done but improper interconnections of the block.	The functional block diagram is done with proper interconnections of the block but not according to specs.	The functional block diagram is done with proper interconnections of blocks according to specs.
	2	Integrating the functional blocks, debugging details and Partial demonstration of results	5	Functional blocks are not identified. No results	Functional blocks are implemented but improper integrated Code/Simulation results are not proper.	Functional blocks are implemented with proper integration. Code/Simulation results are proper but unable to demonstrate.	Proper integration of functional blocks and debugging details are provided. Able to demonstrate the required result.

	3	Plan and need for optimization	5	Not done	Partial	Incomplete	Done
	4	Draft a copy of the project report	5	Not done	Partial	Incomplete	Done
R4	1	Implementation, demonstration, and analysis of results.(Pre optimization and post-optimization discussion)	10	Design is incomplete in terms of specifications and sub-blocks. No results and no analysis	The design of sub-blocks is satisfactory, with partial results but no analysis.	Design is completed in line with the specifications required. Inadequate analysis.	Design is complete, with all functional blocks in working condition. Desired results are obtained and analyzed.
	2	Report submission in Latex (as given in the format)	10	Not followed the recommended format	Followed the format but the contents are not properly organized	Format and contents are satisfactory	The report is properly organized as per the recommended format.
	3	Budget for the project	10	Not done	Partial	Incomplete	Done
	4	Deliver an effective oral presentation	10	Not followed the recommended format	Followed the format but the contents are not properly organized	Format and contents are satisfactory	The report is properly organized as per the recommended format.

End Semester Evaluation (ESA)

A semester-end examination is done based on the rubrics given in Table 3. The semester-end examination includes submission of the project report, demonstration of the projects, and viva-voce conducted by the external and internal examiner. ESAcarries 50% weightage of total marks of projects. The following assessment rubrics are followed to evaluate the student.

Table 2: ESA Rubrics

1	2			3	4		5
Write UP:(W) 10 Marks	Design methodology 20 Marks			Demonstration of results & analysis 10 Marks	Report, presentation & Viva 10 Marks		Total Marks (50)
Objectives, block diagram, operation, results and individual contribution	Design specifications 1. Mathematical /algorithmic 2. Physical	Concepts applied, Optimization techniques	Applications and limitations, Meeting societal/industrial /commercial needs	Representation and analysis of Results	Presentation skills, clarity & language usage	Clear &well organized report	
1.3.1	3.1.6	3.2.2	7.1.2	4.1.3	10.2.2	10.1.3	

Course Code: 19EEEE402	Course Title: Embedded Linux	
L-T-P: 0-0-3	Credits: 03	Contact Hrs: 03
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 03 hrs

Content	Hrs
Unit - 1	
Chapter 01: Introduction to Embedded Linux: A Brief History of Linux -Benefits of Linux -Acquiring and Using Linux -Examining Linux Distributions - Devices and Drives in Linux-Components: Kernel, Distribution, Sawfish, and Gnome.	4 hrs
Chapter 02: Overview of Embedded Linux: Overview: Development-Kernel architectures and device driver model- Embedded development issues-Tool chains in Embedded Linux-GNU Tool Chain (GCC,GDB, MAKE, GPROF & GCONV)-Linux Boot process.	5 hrs
Chapter 03: System Management and user interface: Boot sequence-System loading, sys linux, Lilo, grub-Root file system-Binaries required for system operation-Shared and static Libraries overview-Writing applications in user space-GUI environments for embedded Linux system.	5 hrs
Unit - 2	
Chapter 04: File system in Linux: File system Hierarchy-File system Navigation -Managing the File system –Extended file systems-INODE-Group Descriptor-Directories-Virtual File systems- Performing File system Maintenance - Locating Files –Registering the File systems- Mounting and Unmounting –Buffer cache-/proc file systems-Device special files.	6 hrs
Chapter 05: Configuration: Configuration, Compilation & Porting of Embedded Linux-Examining Shells -Using Variables - Examining Linux Configuration Script Files -Examining System Start-up Files -Creating a Shell Script.	4 hrs
Chapter 06: Process management and Inter process communication: Managing Process and Background Processes -Using the Process Table to Manage Processes - Introducing Delayed and Detached Jobs - Configuring and Managing Services -Starting and Stopping Services -Identifying Core and Non-critical Services -Configuring Basic Client Services - Configuring Basic Internet Services –Working with Modules. IPC-Benefits of IPC- Basic concepts-system calls-creating pipes-creating a FIFO-FIFO operations-IPC identifiers-IPC keys-IPCS commands- Message queues-Message buffer-Kernel Ring Buffer semaphores-semtools-shared memory semtools- signals-sockets.	8 hrs
Unit - 3	
Chapter 07: Linux device drivers: Devices in Linux- User Space Driver APIs- Compiling, Loading and Exporting- Character Devices-Tracing and Debugging- Blocking and Wait Queues- Accessing Hardware- Handling Interrupts-Accessing PCI hardware- USB Drivers- Managing Time- Block Device Drivers- Network Drivers-Adding a Driver to the Kernel Tree.	8 hrs

Text Books (List of books as mentioned in the approved syllabus)

1. Embedded Linux – Hardware, Software and Interfacing - Craig Hollabaugh, Addison-Wesley Professional, 2002
2. Embedded / Real-Time Systems: Concepts, Design and Programming Black Book, New ed (MISL-DT) Paperback – 12 Nov 2003.

References

3. Building Embedded Linux Systems, Karim Yaghmour, First edition, April 2003.
4. Embedded Linux- John Lombardo, Newriders.com

Course Code: 17EEEO402	Course Title: Artificial Intelligence (AI)	
L-T-P 3-0-0	Credits: 3	Contact Hrs: 40
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3 hrs

	Unit – I	
1.	**Introduction** Introduction to AI, What is Intelligence? Characteristics of Intelligence Definitions of AI, History & Evolution of AI, Abilities of AI, Modeling of AI, Application of AI, Adv & Dis Adv of AI	**07 hrs**
2.	**Problem Solving** Problem, Problem Solving, Problem Characteristics, Control Strategies, Problem search strategies, Data Driven & Goal Driven search, State space search, Goal & Game trees, Problem tree and Problem Graph, AND/OR Graph	**08 hrs**
	Unit – II	
3.	**Knowledge and Representation** Introduction, Definition and Importance of Knowledge, Knowledge based systems, Representation of Knowledge, Internal Representation, Prepositional Logic(PL) First order Predicate Logic (FOPL) knowledge organization, knowledge manipulation, acquisition of knowledge	**08 hrs**
4.	**Structured Representation** Structured representation, Graphical representation, IS-ISPART Tree, Associative Network, Conceptual Graph, Linear Graph, Semantic Networks, Frames, Object Oriented Structure, Similarity Nets, Scripts	**07 hrs**
	Unit – III	
5.	**AI Programming languages** AI programming languages, Introduction to LISP: elements of LISP, Introduction to PROLOG and other programming languages.	**05 hrs**
6	**Applications of AI** Matching Techniques, Visual Image Processing, Pattern Recognition and Expert Systems.	**05 hrs**

Books	
1	*"Introduction to Artificial Intelligence and Expert systems"* by D.W Patterson, Printice Hall of India, 1992.
Reference Books:	
1	*"Artificial Intelligence"* by Rich Elaine & Kevin Knight, Tata Mc Graw Hill, 1991.
2	*"Principles of Artificial Intelligence"* by Nils J Nilson, Berlin Springer- Verlag, 1980

Laboratory Title: **Capstone Project**	Lab. Code: 2**1EEEW402**
Total Hours: **50**	Duration of ESA Hours: 2
ESA Marks: **50**	ISA Marks: **50**

Capstone Project Guidelines

(I) Preamble

A project work essentially gives the students a platform to integrate the concepts studied during the study, enhance their analytical capabilities and develop abilities to effectively communicate technical information in multiple formats. During the course of projects, students are asked to follow the research methodology in identifying a problem of their interest though literature survey, carry-out feasibility study, formulate the problem, develop mathematical models, select suitable solution technique etc. Students are also encouraged to develop new formulations, alternate solution techniques, study and apply new optimization algorithms, develop new simulation models and use modern engineering/simulation tools.

(II) Project batch and Guide

Each project batch consists of 4 students. Students will be informed to form their own batch based on the kind of project work and their interest. Each batch is supposed to give four faculty names as guides based on faculty expertise in the order of their preference. Guides will be allocated based on the preference given by the batch. The primary role of the guide is to supervise the work, give appropriate guidance in successfully carrying out the project work.

(III) Project implementation

The principal steps in carrying out the project work are summarized below:

Step-1: Selection of a specialized area for the project work

A specialized area in which the project work is to be carried out depends on the interest and specialized skills acquired by the project team. This includes areas such as power system analysis, power system dynamics, renewable energy, electric drives, VLSI & Embedded system, Power quality issues etc. The proposed work may include simulation studies, hardware implementation or both.

Step-2: Selection of topic based on literature survey

A literature survey in the selected specialized area is to be carried out in order to understand the state of the current research. Further, a critical review of the collected literature will facilitate to summarize key observations. Key observations will lead to identify a specific problem for the project work in terms of alternate/new solution techniques, possible improvements, new formulations or models, hardware implementations etc.

Step-3: Prepare a synopsis

A synopsis highlights the definition of identified problem and its significance. The synopsis will also contain detailed literature review giving the state of the current research on the selected specialized area. It will also brief the problem formulation, solution methodology, tools employed and possible outcomes.

Step-4: Project implementation

The work is to be carried out in phase wise manner, testing or analyzing the partial results obtained. Guide will periodically monitor the progress of the work done giving suitable suggestions as required.

(IV) Schedule

Sl. No.	Activity	Week No.	Evaluation Objectives
1	Announcement to form the batches	At the end of the previous 7th sem	NA
2	Allotment of guides	1st- 2nd	NA
3	Submission of Synopsis	4th- 5th	Literature review, problem formulation, methodology by respective Guides
4	Review-I	8th	Literature review, problem formulation, methodology, tools used in the presence Review Committee
5	Review-II	13th	Implementation and analysis done
6	Review-III	16th	Completion along with Hardware/ Software/ Report. Results and Conclusions.

(V) Evaluation

Evaluation of the project work carried out by each batch will be reviewed periodically by a review committee. Review committee consists of guide and two/ three other faculty members who are guiding other batches. Generally, two to three reviews will be held during a semester. However, each project batch will be supervised by the guide on a weekly basis. Review committee will evaluate for 40% and guide will evaluate for 60% of the total marks.

Activity	Assessment	Marks
ISA (50%)	Project Review committee	30
	Evaluation by Project Guide	20
ESA (50%)	Using ESA Rubrics	50
	Total	**100**

Passing: 40% both in ISA and ESA