Change summary between 2015-16 and 2016-17 admitted batches (i.e. 2015 to 19 batch 2016 to 20 batch)

Program: III Semester Bachelor of Engineering (Electronics & Communication Engineering)			**Teaching Hours**
Course Title: Digital Circuits		**Course Code: 17EECC203**	
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3Hrs/week**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 42 Hrs	**Examination Duration: 3 Hrs**		
Unit-I **Chapter No. 1. Logic Families** Logic levels, output switching times, fan-in and fan-out, comparison of logic families			**03**
Chapter No. 2. Principles of Combinational Logic Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4 variables, Incompletely specified functions(Don't care terms),Simplifying Maxterm equations, Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime Implicant Tables.			**07**
Chapter No. 3. Analysis and design of combinational logic General approach, Decoders-BCD decoders, Encoders, Digital multiplexers- Using multiplexers as Boolean function generators. Adders and subtractors-Cascading full adders, Look ahead carry adders, Binary comparators.			**08**
Unit-II **Chapter No. 4.Introduction to Sequential Circuits** Basic Bistable Element, Latches, A SR Latch, Application of SR Latch, A Switch De bouncer, The SR Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop, Edge Triggered Flip- Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop; Characteristic Equations			**08**
Chapter No. 5. Analysis of Sequential Circuits Registers and Counters, Binary Ripple Counters, Synchronous Binary counters, Ring and Johnson Counters, Design of a Synchronous counters, Design of a Synchronous Mod-n Counter using clocked JK Flip-Flops Design of a Synchronous Mod-n Counter using clocked D, T or SR Flip-Flops.			**08**
Unit-III **Chapter No. 6. Sequential Circuit Design** Introduction to Sequential Circuit Design, Mealy and Moore Models, State Machine notations, Synchronous Sequential Circuit Analysis, Construction of state Diagrams and counter design.			**04**

Chapter No. 7. Introduction to memories Introduction and role of memory in a computer system, memory types and terminology, Read Only memory, MROM, PROM, EPROM, EEPROM, Random access memory, SRAM, DRAM, NVRAM.	**04**

Text Books

1. Donald D Givone, Digital Principles and Design, Tata McGraw Hill Edition,2002
2. John M Yarbrough, Digital Logic Applications and Design, Thomson Learning,2001
3. A Anand Kumar , Fundamentals of digital circuits, PHI,2003

References

1. Charles H Roth, Fundamentals of Logic Design, Thomson Learning, 2004 2.Zvi Kohavi, Switching and Finite Automata Theory, 2nd, TMH
2. .R.D. Sudhaker Samuel, Logic Design, Sanguine Technical Publishers, 2005
3. .R P Jain, Modern Digital Electronics, 2nd, Tata McGraw Hill , 2000

Program: III Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Engineering Design		**Course Code: 17EECF201**	
L-T-P: 0-0-3	**Credits: 3**	**Contact Hours: 03 Hrs/week**	
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**	
Teaching Hours:	**Examination Duration: 2 Hrs**		
PART A			
Planning Introduction to Engineering Design, Problem Definition, Design attributes Gantt Chart, Design Objectives, Design Specifications			**02**
Conceptual Design Functional Analysis, Concept generation, Concept Evaluation			**03**
System Level Design Product Architecture, Configuration Design, Parametric Design			**03**
Detail Design Sub-system Design, Design Verification			**03**
PART B			
OrCAD Functional simulation of basic Analog and Digital application circuits using OrCAD eCAD tool			**01**
Schematic Capture of the reference design using using OrCAD eCAD tool.			**01**
Layout Design of the reference design using using OrCAD eCAD tool.			**01**
Creation of Symbols/Cell/Part			**01**
LabVIEW Introduction to LabVIEW and functional simulation of basic Analog and Digital application circuits in LabVIEW			**01**
Functional Simulation of the circuit for selected problem statement			**01**
Co-simulation of the circuit for selected problem statement.			**01**

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)			**Teachig Hours**
Course Title: Linear Integrated circuits		**Course Code:17EECC205**	
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3Hrs/week**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 40Hrs	**Examination Duration: 3 Hrs**		**Hrs**

Unit I	
Chapter No 1. OPAMP characteristics Ideal and non-ideal OPAMP terminal characteristics, Input and output impedance, output Offset voltage, Small signal and Large signal bandwidth.	**04**
Chapter No 2. OPAMP with Feedback OPAMP under Positive and Negative feedback, Impact Negative feedback on Bandwidth, Input and Output impedances, Offset voltage under negative feedback, Follower property & Inversion Property under linear mode operation.	**04**
Chapter No 3. Basic OPAMP architecture Basic differential amplifier, Common mode and difference mode gain, CMRR, 5-pack differential amplifier with design, 7-pack operational amplifier, Slew rate limitation, Instability and Compensation, Bandwidth and frequency responsecurve.	**08**
Unit II	
Chapter No 4. Current Mirrors Current Mirror circuits and Modeling, Figures of merit (output impedance, voltage swing), Widlar, Cascode and Wilson current Mirrors, Current source and current sink.	**08**
Chapter No 5. Linear applications of OPAMP DC and AC Amplifier, Summing, Scaling and Averaging amplifiers (Inverting, Non-inverting and Differential configuration), Integrator, Differentiator,Voltage sources, current sources and current sinks, Active Filters –First and second order Low pass & High pass filters. V to I and I to V converters.	**08**
Unit III	
Chapter No 6 . Nonlinear applications of OPAMP Zero Crossing detectors (ZCD. Comparator), Inverting Schmitt trigger circuits, Triangular/rectangular wave generators, Waveform generator, Precision rectifier, Limiting circuits, Clamping circuits, Peak detectors, sample and hold circuits, Phase shift oscillator, Wein bridge oscillator, DAC and ADC	**08**

Text Book

1. Behzad Razavi, Fundamentals of microelectronics , 2nd edition.
2. Phillip E. Allen, Douglas R. Holberg, CMOS Analog CircuitDesign.
3. Ramakant A. Gayakwad, Op - Amps and Linear IntegratedCircuits.

References

1. A.S. Sedra& K.C. Smith, MicroelectronicCircuits,
2. Sergio Franco, Design with Operational Amplifiers and Analog IntegratedCircuits.
3. David A. Bell, Operational Amplifiers and LinearIC's.
4. B. Razavi, Design of Analog CMOS Integrated Circuits McGraw-Hill,2001

Semester: IV

Course Title: **Product Realization**	Course Code: 17EECF203
Total Contact Credits: **2** **(0-0-2)**	Duration of SEE Credits: -
ISA Marks: 80	ESA Marks: 20

Week #	Particulars	Template #	Venue
Week 1 **and** **Week 2**	➢ Introduction to Prototyping ➢ Defining- Specifications, Part Drawings, Assembly Drawings, PCB Layout, Wireframe , Pseudocode, BOM, Process Plan, Fabrication and Test Plan Validation ➢ IOT Workshop		Studio Engagement
Week 3	➢ Identifying sub-assemblies (minimum of 3) ➢ Selection of materials for all the parts and joining techniques		Makers Space/
Week 4	➢ Process plan ➢ Identifying the proper machines and tools required for prototyping. ➢ Preparing of raw materials for prototyping. ➢ Plan and procure the bought out parts.		
Week 5	➢ Fabricate the parts for sub assembly 1		
Week 6	➢ Fabricate the parts for sub assembly 2		
Week 7	➢ Fabricate the parts for sub assembly 3		
Week 8	➢ Assemble the sub assemblies and check for interference and functionality		
Week 9	➢ Test the functional prototype using proper identified test methods.		

Week 10	➢ Analyse the test results ➢ System modification		
Week 11	➢ Final concluding review ➢ Product catalogue		Studio/ Makers Space

References

1. Pahl, G., Beitz, W., Feldhusen, J. and Grote ; "Engineering Design-A Systematic Approach" by, K.-H- Springer; 3rd ed. 2007

Course Title: **Embedded Intelligent Systems**		Course Code: 17EECE310
L-T-P: 0-0-3	Credits: 3	Contact Hrs: **6hrs/week**
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hrs: 60	Exam Duration: 3 hrs	

	Unit - I	
1	**Basics of embedded systems** Linux Application Programming, System V IPC, . Linux Kernel Internals and Architecture , Kernel Core , Linux Device Driver Programming, Interrupts & Timers , Sample shell script, application program, driver source build and execute	**10 hrs**
2	**Heterogeneous computing** Basics of heterogeneous computing with various hardware architectures designed for specific type of tasks, Advanced heterogeneous computing with a. Introduction to Parallel programming b.GPU programming (OpenCL). Open standards for heterogeneous computing (Openvx) , Basic OpenCL examples - Coding, compilation and execution	**12 hrs**
	Unit - II	
3	**ML Frameworks with the target device** Caffe, tensorflow, TF Lite machine learning frameworks & architecture ,Model parsing, feature support and flexibility ,Supported layers , advantages and disadvantages with each of these frameworks, Android NN architecture overview , Full stack compilation and execution on embedded device	**16 hrs**
4	**Model Development and Optimization** Significance of on device AI ,Quantization , pruning, weight sharing, Distillation ,Various pre-trained networks and design considerations to choose a particular pre-trained model ,Federated Learning , Flexible Inferencing	**8 hrs**
	Unit - III	
5	**Android Anatomy** Android Architecture ,Linux Kernel , Binder , HAL Native Libraries , Android Runtime, Dalvik Application framework , Applications, IPC	**8 hrs**

Text Books

1. Linux System Programming , by Robert Love , Copyright © 2007 O'Reilly Media
2. Heterogeneous Computing with OpenCL, 2nd Edition by Dana Schaa, Perhaad Mistry, David R. Kaeli, Lee Howes, Benedict Gaster , Publisher: Morgan Kaufmann

Reference Books:

1. Deep Learning , MIT Press book ,Goodfellow, Bengio, and Courville's
2. Beginning Android , by Wei-Meng Lee , Publisher: Wrox , O'Reilly Media

Scheme for End Semester Assessment (ESA)

UNIT	Experiments to be set of 10 Marks Each	Chapter Numbers	Instructions
I	Project Examination	1,2,3,4,5	Project implementation and demonstration 20 marks

Course Code: 19EECE416	Course Title: Biosensor	
L-T-P: 0-0-3	Credits: 3	Contact Hrs: 72
ISA Marks: 00	ESA Marks: 100	Total Marks: 100
Teaching Hrs: 72		Exam Duration: 3 hrs

Content	Hrs
Unit - 1	
Chapter No. 1. Basic Introduction to sensors Introduction to sensors: fundamental characteristics such as Sensitivity, linearity, repeatability, hysteresis, drift. Sensing Principles: optical sensors, electrochemical sensors, micromechanical sensors, surface Plasmon sensors, colorimetric Sensors, acoustic sensors	5 hrs
Chapter No. 2. Active Electrical Transducers Thermoelectric transducers, thermoelectric phenomenon, common thermocouple systems, piezoelectric transducers, piezoelectric phenomenon piezoelectric materials, piezoelectric force transducers, piezoelectric strain, piezoelectric torque transducers, piezoelectric pressure transducers, piezoelectric acceleration transducers. Magnetostrictive transducers Magnetostrictive force transducers, Magnetostrictive acceleration transducers, Magnetostrictive torsion transducers, Hall Effect transducers, and application of Hall transducer. Electromechanical transducers-Tachometers, variable reluctance tachometers Electrodynamic vibration transducers, Electromagnetic pressure electromagnetic flowmeter. Photoelectric transducers- photoelectric phenomenon, photoelectric transducers, Photo volatile transducers, Photo emissive transducers. Electrochemical transducers- basics of electrode potentials, reference electrodes, indicator electrodes, measurement of PH, measurement of bioelectric signals.	10 hrs
Unit - 2	
Chapter No. 3. Passive electrical transducer Introduction, Resistive transducers- resistance thermometers, hot wire resistance transducers, Resistive displacement transducer, Resistive strain transducer, resistive pressure transducer, resistive optical radiation transducers. Inductive transducers-Inductive thickness transducers, Inductive displacement transducers, Movable core-type Inductive transducers, eddy current type Inductive transducers. Capacitive transducers-Capacitive thickness transducers, capacitive displacement transducers, capacitive moisture transducers Substrate and Wafers, Active Substrate Materials, Silicon as Substrate Material, Silicon Compounds, Silicon Piezo resistors, Gallium Arsenide, Quartz, Piezoelectric Crystals, Polymers, Packaging Materials.	5 hrs
Chapter No. 4. Microfabrication Technology Design of process flow for device fabrication for application in biology and medicine: Introduction to the Clean room and contaminants, Wafer cleaning processes (DI water, RCA, metallic impurities, etc.), Substrate materials: Silicon,	10 hrs

polymer and PCB, Thermal oxidation: Wet and dry oxidation, thin film deposition techniques: PVD- DC and RF Magnetron Sputtering, thermal evaporation, e-beam evaporation, LPCVD, PLD. Types of masks: Hard and soft Lithography, Lithography – UV Photolithography, Soft lithography, additive manufacturing. Mask design and fabrication – Photo resists and mechanical mask such as stencils. Types of etching- Wet etching- anisotropic and Isotropic and dry etching RIE and DRIE. Device fabrication and inspection in the clean room.	
Unit - 3	
Chapter No. 5. Biosensors Introduction: Biosensors and its applications in health care, agriculture, drug discovery and environmental monitoring. Devices for biology and medicine: Microfluidic channels, flow cytometry/ sorting, microchip using electrophoresis, force measurement with cantilevers, micro engineered devices for medical therapeutics, blood pressure sensors, devices for drug delivery, and devices for minimally invasive surgery.	5 hrs
Chapter No. 6. Biological components for detection Enzymes, antigen-antibody reaction, biochemical detection of analysts, organelles, whole cell, receptors, DNA probe, pesticide detection, sensors for pollutant gases. Surface chemistry: Immobilization of biorecognition element, Antigen-Antibody functionalization, and assay labels including radioisotopes, fluorophores, dyes.	5 hrs

Text Books (List of books as mentioned in the approved syllabus):

1. Fundamentals of Microfabrication and Nanotechnology by Marc J. Madou, 3rd edition. Taylor and Francis group.
2. Transducers and Instrumentation – D.V.S. Murthy, 2nd Edn, PHI Ltd, 2010.
3. A.P.F. Turner, I. Karube & G.S. Wilson: Biosensors: Fundamentals & Applications, Oxford University Press, Oxford, 1987.

References:

1. Ernest O. Doeblin : Measurement Systems, Application and Design, McGraw-Hill, 1985.
2. Richard S.C. Cobbold : Transducers for Biomedical Measurements: Principles and Applications, John Wiley & Sons, 1974
3. John G. Webster (ed.) : Medical Instrumentation - Application and Design; Houghton Mifflin Co., Boston, 1992.
4. Stephen D. Senturia : "Micro system Design", Kluwer Academic Publishers, 2001

KLE TECH. Earlier known as B. V. B. College of Engineering & Technology	School of Electronics & Communication Engineering

Course Code: 19EECE402	Course Title: Information Theory and Coding	
L-T-P-SS: 2-0-1	Credits: 3	Contact Hrs: 40
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3 hrs

Content	Hrs
Unit - 1	
Chapter No. Chapter 1:Information Theory: Information Theory: Introduction, Measure of information, Average information content of symbols in long independent sequences, Average information content of symbols in long dependent sequences. Mark-off statistical model for information source, Entropy and information rate of mark-off source	7 hrs
Chapter No. Chapter 2: Source Coding: Encoding of the source output, Shannon's encoding algorithm. Communication Channels, Discrete communication channels, Continuous channels. Source coding theorem,, Huffman coding	8 hrs
Unit - 2	
Chapter No. Chapter 3: Channel coding Discrete memory less Channels, Mutual information, Channel Capacity Channel coding theorem, Differential entropy and mutual information for continuous ensembles, Channel capacity Theorem.	4 hrs
Chapter No. Chapter 4: Introduction to Error Control Coding: Introduction, Types of errors, examples, Types of codes Linear Block Codes: Matrix description, Error detection and correction, Standard arrays and table look up for decoding.	7 hrs
Chapter No. Chapter 5: Binary Cycle Codes Algebraic structures of cyclic codes, Encoding using an (n-k) bit shift register, Syndrome calculation.	4 hrs
Unit - 3	
Chapter No. Chapter 6: BCH codes RS codes Golay codes, Shortened cyclic codes, Burst error correcting codes. Burst and Random Error correcting codes. Convolution Codes, Time domain approach. Transform domain approach. Systematic Convolution codes	10 hrs

Text Book (List of books as mentioned in the approved syllabus)

1. K. Sam Shanmugam, Digital and analog communication systems, John Wiley, 1996

2. Simon Haykin, Digital communication, John Wiley, 2003

References

1. Ranjan Bose, ITC and Cryptography, TMH(reprint 2007), 2002

2. Glover and Grant, Digital Communications , 2, Pearson, 2008
3. D Ganesh Rao, K N Haribhat, Digital Communications, Sanguine, 2009

Course Title: **CMOS ASIC Design**	Course code: 18EECE420	
L-T- P: 0-0-3	Credits: 03	Contact Hrs: 06hrs/week
CIE Marks: 100	SEE Marks: 00	Total Marks: 100
Teaching Hrs: 16hrs Lab Hrs: 24 hrs		

Chapter No. 1. Introduction: Design of combinational and sequential logic gates in CMOS. Layout and characterization of standard cells. Verilog for representing gate level netlists.	8 hrs
Chapter No. 2. Timing Analysis: Sequential circuit timing and static timing analysis. Cell and net delays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock Domains	10hrs
Chapter No. 3: Physical design Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew.	12 hrs
Chapter No. 4. Standard Data formats: Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes.	6 hrs
Chapter No. 5. Packaging An overview of package design and implementation and system level timing.	4 hrs

Reference Books:

1. The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985.
2. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime, 2nd edition, 2001.
3. Static Timing Analysis for Nanometer Designs A Practical Approach, J. Bhasker • Rakesh Chadha, Springer Science+Business Media, LLC 2009

Tools: Cadence Innovous, Encounter

Course Title: **Physical Design-Analog**	Course code: 18EECE419	
L-T- P: 0-0-3	Credits: 03	Contact Hrs: 06hrs/week
CIE Marks: 100	SEE Marks: 00	Total Marks: 100
Teaching Hrs: 16hrs Lab Hrs: 24 hrs		

Chapter No 1. Standard cell Layout creation Layout Practice Sessions (DRC/LVS Dirty layout), Understanding verification errors, Error debugging skills, Hands on experience of using layout editor, Quality of the layout, Half DRC rules, Mega module creation.	8 hrs
Chapter No 2. Analog layout Importance of performance in Analog layout, Importance of floor planning and placement, Attributes need to be taken care during routing stage, Introduction to DRC, LVS, Density and RCX.	8 hrs
Chapter No 3. Matching and Guard rings, Matching: Introduction to mismatch concepts, Causes for mismatch, Types of mismatch, Rules for matching, Activities. Guard ring : What is guard ring, Usage of guard ring	6 hrs
Chapter No 4. Reliability issues Introduction to failure mechanism, Causes of reliability issues, Process enhancement techniques and Layout considerations to reduce reliability issues	8 hrs
Chapter No 5. Physical design of amplifier and buffer Applying the studied concepts and doing layout, Prioritising the constraints given, Quality checks, Buddy reviews and implementations, Documentation	10 hrs

Reference:

The Art of Analog Layout – Alan Hastings

CMOS IC layout – Dan Clien

IC Layout Basics – Chris saint and Judy saint

Course Code: **19EECE322 / 19EECE422**	Course Title: **Introduction to Deep Learning**	
L-T-P: **2-0-1**	Credits: **3**	Contact Hrs: **4**
ISA Marks: **50**	ESA Marks: **50**	Total Marks: **100**
Teaching Hrs: **42**		Exam Duration: **3 hrs**

Content	**Hrs**
Unit - 1	
Chapter 1: Introduction to Deep Learning: What is Deep Learning?, Applications of deep learning, Differences between machine learningand deep learning, Basics of Neural Networks, Supervised Learning with Neural Networks, Logistic regression as a neural network, Computation graph, shallow neural networks, Deep neural networks. Introduction to metric tensors and tensorflow, Basic programs in tensorflow.	8 hrs
Chapter 2: Hyper-Parameter Tuning, Regularization and Optimization: Basics of Hyper-parameters, Regularization, Need for regularization, dropout regularization, gradient checking, mini-batch gradient descent, exponentially weighted averages and its biascorrection, Gradient descent with decay, Adam's optimization algorithm, The problem of localminima, weight initialization in neural networks, Normalizing activations in a network, Fitting Batch norm into a network, Softmax regression, Softmax classifier.	8 hrs
Unit - 2	
Chapter 3: Convolutional Neural Networks Introduction to Computer Vision and Image Processing, 2D Convolutions, Strided convolution,convolution over volume, One layer of a convolution network, ReLu and pooling, Example of aConvNet, Classic CNN Networks, ResNet architecture, Inception Networks, Transfer learning,Data Augmentation, Residual networks, Object Localization, Landmark and object detection, Convolutional implementation of sliding windows, YOLO algorithm, Car detection algorithm using YOLO, One shot learning, Face recognition algorithm.	12 hrs
Chapter 4: Recurrent Neural Networks Backpropogation through time, RNN model, Types of RNN, Vanishing gradients with RNN,Gated Recurrent Unit, LSTM, Bidirectional RNN, Deep RNN, basics of NLP and Concept ofword embedding, speech recognition.	04 hrs
Unit - 3	
Chapter 5: Unsupervised Deep Learning Concepts of Unsupervised deep learning, RBM (Restricted Boltzman Machine) and auto encoders, structure of Auto encoders, collaborative filtering with RBM, Deep belief networks.	10 hrs

Change summary between 2016-17 and 2018-19 admitted batches
(i.e. 2016 to 20 batch 2017 to 21 batch)

Laboratory Title: **C Programming (for Diploma)**	Lab. Code: 18EECF204
Total Hours: 20	Duration of Exam: 02
ESA Marks: 20	Total ISA. Marks: 80

Experiment wise plan

1. **List of experiments/jobs planned to meet the requirements of the course.**

Expt./Job No.	Experiment/job Details	No. of Lab. Session/s per batch (estimate)	Marks/Experiment
1.	Write a C program to perform addition , subtraction , multiplication and division of two numbers .	01	8.00
2.	Write a C program to i) Identify greater number between two numbers using C program. ii) To check a given number is Even or Odd .	01	8.00
3.	Write a C program to i) To find the roots of a quadratic equation. ii) Find the factorial of given number.	01	8.00
4.	Write a C program to i) To find the sum of n natural numbers. ii) Print the sum of 1 + 3 + 5 + 7 + + n	01	8.00
5.	Write a C program to i) Print the pattern . * * * * * * * * * * * * * * * ii) Print the pattern 1 1 2	01	8.00

	1 2 3 1 2 3 4 1 2 3 4 5		
6.	Write a C program to To test whether the given character is Vowel or not. (using switch case)	01	8.00
7.	Write a C program to To accept 10 numbers and make the average of the numbers using one dimensional array.	01	8.00
8.	Write a C program to Find out square of a number using function.	01	8.00
9	Write a C program to To find the summation of three numbers using function.	01	8.00
10	Write a C program to Find out addition of two matrices.	01	8.00

1. **Materials and Resources Required:**

Text Book

1. Programming in ANSI C, E Balagurusamy

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)			Lab+ Teaching Hours
Course Title: Data Structures Application Lab		Course Code: 18EECC210	
L-T-P: 0-0-2	Credits: 2	Contact Hours: 4Hrs/week	
ISA Marks: 80	ESA Marks:20	Total Marks: 100	
Teaching + Lab. Hours: 48 Hrs	Examination Duration:2 Hrs		

1.	**Hashing** Hash, Hash function, Hash Table, Collision resolution techniques, Hashing Applications	12Hrs
2.	**Trees** Computer representation, Tree properties, Binary Tree properties, Binary search trees properties and implementation, Tree traversals, AVL tree, 2-3 Tree	20Hrs
3.	**Graphs** Computer representation, Adjacency List, Adjacency Matrix, Graph properties, Graph traversals	16Hrs

Book

1. Data Structures A Psedocode Approach with C, Richard F. Gilberg & Behrouz A. Forouzan, second edition, CENGAGE Learning.
2. Data Structures Using C. Author, Aaron M. Tenenbaum. Publisher, Pearson Education.

Course Code: **19EECC302**	Course Title: OOPS using C++	
L-T-P: 2-0-1	Credits: 3	Contact Hrs: 42
ISA: Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hrs: 42		Exam Duration:

Content	**Hrs**
Unit - 1	
Chapter 1: Fundamental concepts of object oriented programming: Introduction to object oriented programming, Programming Basics (keywords, identifiers, variables, operators, classes, objects),Arrays and Strings Functions/ methods (parameter passing techniques),	04 hrs
Chapter 2: OOPs Concepts: Overview of OOPs Principles, Introduction to classes & objects ,Creation & destruction of objects, Data Members, Member Functions , Constructor & Destructor , Static class member, Friend class and functions, Namespace	08hrs
Unit - 2	
Chapter 3: Inheritance: Introduction and benefits, Abstract class, Aggregation: classes within classes Access Specifier, Base and Derived class Constructors, Types of Inheritance. Function overriding	8 hrs
Chapter 4: Polymorphism: Virtual functions, Friend functions, static functions, this pointer	6 hrs
Unit - 3	
Chapter 5: Exception Handling: Introduction to Exception, Benefits of Exception handling, Try and catch block, Throw statement, Pre-defined exceptions in C++,Writing custom Exception class	8 hrs
Chapter 6: I/O Streams: C++ Class Hierarchy, File Stream, Text File Handling, Binary File Handling Error handling during file operations, Overloading << and >> operators	6 hrs

Books/References: **Text Book** **1. Robert Lafore, "Object oriented programming in C++", 4th Edition, Pearson education, 2009.** **References** **1. Lippman S B, Lajorie J, Moo B E, C++ Primer, 5ed, Addison Wesley, 2013.** **2. Herbert Schildt: The Complete Reference C++, 4th Edition, Tata McGraw Hill**	

Change summary between 2018-19 and 2019-20 admitted batches
(i.e. 2017 to 21 batch 2018 to 22 batch)

Program: III Semester Bachelor of Engineering (Electronics & Communication Engineering)			**Teaching Hours**
Course Title: Signals and Systems		**Course Code: 19EECC202**	
L-T-P: 4-0-0	**Credits: 4**	**Contact Hours: 4Hrs/week**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 50Hrs	**Examination Duration: 3 Hrs**		
Unit I			
Chapter No. 01: Signal Representation Definition of a signals and systems, classification of signals,(analog and discrete signal, periodic and aperiodic, deterministic and random signals, even and odd signals, energy and power) , basic operation on signals(independent variable, dependent variable , time scaling, multiplication, time reversal), elementary signals (Impulse, step, ramp, sinusoidal, complex exponential), Systems Interconnections(series, parallel and cascade), properties of linear systems. (homogeneity ,superposition, linearity and time invariance, stability, memory, causality)			**10**
Chapter No. 02 : LTI System Representation Impulse response representation and properties, Convolution, convolution sum and convolution integral. Differential and difference equation Representation, Block diagram representation			**10**
Unit II			
Chapter No. 03:Fourier representation for signals Introduction, Discrete time Fourier series(derivation of series excluded) and their properties. Discrete Fourier transform (derivation of transform excluded) and properties			**10**
Chapter No. 04:Applications of Fourier transform Introduction, frequency response of LTI systems, Fourier transform representation of periodic signals, Fourier transform representation of discrete time signals. Sampling of continuous time signals.			**10**
Unit III			
Chapter No. 05: Z-transform Definition of z-transform, Properties of ROC, Properties of Z-transforms: Inverse z-transforms (Partial Fraction method, long division method), Unilateral Z-transform, Transform of LTI.			**10**
Text Book (List of books as mentioned in the approved syllabus) 1. Simon Haykin and Barry Van Veen , Signals and Systems, Second, John Wiley & Sons,2002 2. Alan V Oppenheim ,Alan S Willsky and S. Hamid Nawab , Signals and Systems, Second, PHI public,1997 **References** 1. H. P Hsu, R. Ranjan, Signals and Systems , TMH,2006			

2. GaneshRaoandSatishTunga,,SignalsandSystems,SanguineT,2004
3. M.J.Roberts, Fundamentals of Signals and Systems, first Edition, TMH

Change summary between 2018-19 and 2019-20 admitted batches
(i.e. 2018 to 22 batch 2019 to 23 batch)

Laboratory Title: **Senior Design Project**	Lab. Code:**20EECW401**
Credit : 0-0-6 Total Hours: 70**hours/week**	Duration of exam: **2 hours**
Total Exam Marks: **100**	ISA Marks: **50**

Application Areas are,

- Smart City
- Connected Cars
- Home Automation
- Health care
- Smart energy
- Automation of Agriculture

Guide lines for selection of a project:

- The project needs to encompass the concepts learnt in the previous semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the defined problem statement of the project work.
- Student can select a project which leads to a product or model or prototype.
- Time plan: Effort to do the project should be between 60-70Hrs per team, which includes self-study of an individual member (80-100 Hrs) and team work (40-50hrs).
- Learning overhead should be 20-25% of total project development time.

Criteria for group formation:

- 3-4 students in a team.
- Role of teammates: Team lead and members.

Allocation of Guides and Mentors for the projects:

Every Project batch will be allocated with one faculty.

Details of the project batches:

- Number of faculty - members: 50
- Number of students:3-4 students in a team.

Role of a Guide

The primary responsibility of the guide is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, guide should help towards its successful completion as per the predefined standards.

How student should carry out a project:

- Define the problem.
- Specify the requirements.
- Specify the design in the understandable form (Block Diagram, Flowchart,Algorithm,etc).
- Analyze the design and identify hardware and software componentsseparately.
- Select appropriate simulation tool and development board for the design.
- Implement the design.
- Optimize the design and generate the results.
- Result representation and analysis.
- Prepare a document and presentation.

Report Writing

- The format for report writing should be downloaded from ftp://10.3.0.3/projects
- The report needs to be shown to guide and committee for each review.
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Evaluation Scheme

- Internal semester assessment (ISA)
- Evaluation is done based on the evaluation rubrics given in Table 1
- Project shall be reviewed and evaluated by the concerned Guide for 50% of the marks.
- Project shall be evaluated by the review committeefor 50% of the marks.