KLE Technological University — Creating Value, Leveraging Knowledge	School of Electronics & Communication Engineering **PG – VDES**

Program: Digital Electronics			
Course Title: Principles and Practices of Engineering Education		**Course Code:** 15ECRC701	
L-T-P: 2-0-1	**Credits: 3**	**Contact Hours: 3**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 40	**Examination Duration: 3 hrs**		
1. **Fundamental Principles of Teaching and Learning** 2. **Learning Styles and Theories** 3. **Instructional Design Models and Technology Enhanced Learning** 4. **Assessment and Evaluation** 5. **Engineering Learning Modules**			**8 Hours** **8 Hours** **8 Hours** **8 Hours** **8 Hours**

Program: Digital Electronics			
Course Title: Data Structure using C		**Course Code:** 17EVEC701	
L-T-P: 0-0-1	**Credits: Audit**	**Contact Hours: 2**	
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**	
Teaching Hours: 25	**Examination Duration: -**		
Chapter 01:C language features Pointers revisited, Strings, Structures – Basics, Structures and functions, Arrays of structures, Pointers to structures, Self Referential Structures, Unions and bit fields, Files.			5 Hrs
Chapter 02:Stacks and Queues Definition, Representation and Applications of stack. Definitions, representation and applications of linear, circular, queues, multiple queues, priority queue. Recursion			5 Hrs
Chapter 03:Lists Linked lists, singly, doubly, circular lists, definitions, representations. Implementation of list operations, applications – polynomial addition, addition of long integers. Linked stacks, Linked Queues			5 Hrs
Chapter 04:Trees Binary trees – Definitions, traversals (recursive and iterative versions), Building and searching, Threaded Binary trees, Trees and their applications			5 Hrs
Exchange sorts, Selection and tree sorts, Merge and radix sorts			5 Hrs
Text Book 1. Aaron M. Tenenbaum, et al, Data Structures using C, II Edition, PHI, 2006 2. Horowitz, Sahani, Anderson-Feed, Fundamentals of Data Structures in C, II Edition, University, 2008 **References** 1. E Balaguruswamy, The ANSI C programming Language, II Edition, PHI, 2010 2. Yashavant Kanetkar, Data Structures through C, II Edition, BPB public, 2010 3. Richard F. Gilberg, Behrouz A. Forouzan , Data Structures: A Pseudocode Approach With C, II Edition, Course Tec, 2009			
Lab: **1.** Programs on Pointer concepts. **2.** Programs on string handling functions, structures union And bit-files.			

3. Programming on files **4.** Programming on stacks data structures **5.** Programs on implementation of different queue data structures. **6.** Programs on implementation of different types of Linked lists **7.** Programs on Implementation of trees **8.** Programs to implement different sorting techniques. **9.** Programming on graph **10.** Programming on hashing tables **11.** Design and implement stack queue data structures **12.** Design and implement linked list data structures **13.** project	

Program: I Semester Master of Technology (Digital Electronics)			**Teaching Hours**
Course Title: Principles of Embedded Systems		**Course Code: 17EVEC703**	
L-T-P: 0-0-2	**Credits: 2**	**Contact Hours: 4 Hrs/week**	
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**	
Teaching Hours: 42 Hrs	**Examination Duration:**		
1. Introduction to embedded system: Introduction, Classification of Embedded System, Major Application Areas, Purpose of Embedded System. Characteristics and quality attributes of Embedded Systems, Design Metric and Optimizing the metrics.			**06 Hrs**
2. Typical Embedded Systems: Core of Embedded System-processor fundamentals, up vs uc, risc vs cisc, vonneumann vs Harvard, 8051 controller architecture and programmer model, Memory, Sensor and Actuators, Communication Network, Embedded Firmware			**08 Hrs**
3. Low Level programming Concepts: Addressing Modes, Instruction Set and Assembly Language programming(ALP), Developing, Building, and Debugging ALP's			**08 Hrs**
4. Middle Level Programming Concepts: Cross Compiler, Embedded C language implementation, programming, & debugging, Differences from ANSI-C, Memory Models, Use of directives, Functions, Parameter passing and return types			**02 Hrs**
5. On-Chip Peripherals Study, Programming, and Application: Ports: Input/Output, Timers & Counters, UART, Interrupts			**08 Hrs**
6. External Interfaces Study, Programming and Applications : LEDS, Switches(Momentary type, Toggle type), Seven Segment Display: (Normal mode, BCD mode, Internal Multiplexing & External Multiplexing), LCD (8bit, 4bit, Busy flag, custom character generation), Keypad Matrix, Stepper Motor, DC Motor			**10 Hrs**

Text Books

1. Introduction to Embedded Systems 1E by Shibu K V.
2. Kenneth J. Ayala ; "The 8051 Microcontroller Architecture, Programming & Applications" 2e, Penram International, 1996 / Thomson Learning 2005
3. Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; "The 8051 Microcontroller and Embedded Systems – using assembly and C "- PHI, 2006 / Pearson, 2006

References

1. Embedded System Design: A Unified Hardware/Software Introduction – Frank Vahid, Tony Givargis, John Wiley & Sons, Inc.2002
2. Predko ; "Programming and Customizing the 8051 Microcontroller" –, TMH
3. Raj Kamal, "Microcontrollers: Architecture, Programming, Interfacing and System Design", Pearson Education, 2005

Program: I Semester Master of Technology (Digital Electronics)			**Teaching Hours**
Course Title: RISC Architectures		**Course Code: 17EVEC705**	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 3 Hrs/week**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 46 Hrs	**Examination Duration:**		
1. The 32 bit RISC Architecture: The Acorn RISC machine, Architectural inheritance, Architecture of ARM7TDMI, ARM programmers model, ARM development tools, 3 stage pipeline ARM organization, ARM instruction execution.			**06 Hrs**
2. 32 bit Instruction set: Data processing instruction, Branch instruction, Load store instruction, Software interrupt instruction, Program status register instruction, Conditional execution, Example programs, 16bit Instruction set-The Thumb programmer model, ARM-Thumb interworking, other branch instructions, Data processing instructions, Single/Multiple register load store instruction, Stack operation, Software interrupt instructions, example programs.			**06 Hrs**
3. Exception Handling: Introduction, Interrupts, error conditions, processor exception sequence, the vector table, Exception handlers, Exception priorities, Procedures for handling exceptions.			**04 Hrs**
4. Memory Hierarchy Design: Cache basics, Miss rate and penalty, Cache Hierarchy, Memory Organizations, Memory Hierarchy.			**06 Hrs**
5. Pipelining: Linear pipeline processor, Nonlinear pipeline processor, Instruction pipeline design, Branch handling techniques, Arithmetic pipeline design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipeline.			**08 Hrs**
6. Cortex M4 : Functional description, programmer's model, memory protection unit, nested vectored interrupt controller.			**06 Hrs**
7. Multi-Core Architectures : Introduction to Intel Architecture, How an Intel Architecture System works, Basic Components of the Intel Core 2 Duo Processor: The CPU, Memory Controller, I/O Controller.			**07 Hrs**
8. Current Trends in Intel Architectures and Applications : Seminar on current trends in Intel Architectures			**03 Hrs**

Text Books

1. "ARM System- on-Chip Architecture" by 'Steve Furber', LPE, Second Edition.
2. "ARM Assembly Language fundamentals and Techniques" by William Hohl, CRC press, 2009.
3. D. A. Patterson and J. L. Hennessey "Computer Organization and Design", Morgan , Kaufmann,2002
4. H. Jonathan Chao and Bin Liu, "High performance switches & routers", Wiley Interscience, 2007.
5. Kai Hwang, " Advanced Computer Architecture – TMH – 1993
6. Web resources for Example Architectures of INTEL and Texas Instruments: http:/ /download.intel.com/design/intarch/papers/321087.pdf

References

1. Kai Hwang, Faye A. Briggs, Computers Architecture and Parallel Processing – MGH – 1985
2. David E Culler, Jaswinder Pal Singh, Anoop Gupta "Parallel Computer Architecture", Harcourt Asia Pte Ltd 2000
3. Stalling W." Computer Organization and Architecture- Designing for performance" PHI,2005
4. D. Sima,T. Fountain, P.Kasuk," Advanced Computer Architecture-A Design Space Approach" Addisson Wesley,1997.
5. M. J. Flynn,"Computer Architecture, Pipelined And Parallel Processing", Narosa Publications, 1998.

List of Experiments:

1. Write an ALP to verify data transfer w.r.t memory to achieve following
   i. 8 bit data transfer
   ii. 16 bit data transfer
   iii. 32 bit data transfer
2. Write an ALP for Tables and lists to do following:
   i. Add an entry to a list
   ii. Remove an element from the queue
3. Write an ALP to pass parameters to a subroutine.
   i. Ascending order
   ii. Descending order
4. Write a 'C' program & demonstrate an interfacing of Alphanumeric LCD 2X16 panel to LPC2148Microcontroller
5. Write a 'C' program & demonstrate concept of Interrupts interface to LPC2148 Microcontroller.
6. Write a 'C' program & demonstrate an interfacing of DAC to LPC2148 Microcontroller.
7. Write a 'C' program & demonstrate an interfacing of UART to LPC2148 Microcontroller.
8. Write a 'C' program & demonstrate an interfacing of ADC to LPC2148 Microcontroller.
9. Write a 'C' program & demonstrate an interfacing of RTC to LPC2148 and read time, date and year.
10. Write a 'C' program & demonstrate interface I2C to LPC2148
11. Develop a code for college bell system. (Use the following interfaces LCD, RTC and Buzzer).

Reference Books

1. "ARM System- on-Chip Architecture" by 'Steve Furber", LPE, Second Edition.
2. "Embedded Systems- Architecture, Programming and Design" by Raj Kamal, TMH
3. Dr. K.V.K.K. Prasad, "Embedded/Real-time systems: concepts, Design & Programming", published by dreamtech press.

Manual

1. LPC2148 datasheet by NXP.
2. LPC2148 board manual by ALS, Bangalore.

Program: Digital Electronics			**Teaching Hours**
Course Title: Electronic System Design		**Course Code: 17EVEC707**	
L-T-P: 0-0-3	**Credits: 3**	**Contact Hours:6 Hrs/week**	
ISA Marks: 100	**ESA Marks:**	**Total Marks: 100**	
Teaching Hours: 25 Hrs	**Examination Duration: --**		
To level specifications, Block level specifications, Timing of micro architecture, Verification and test plan, Schematic capture			05 Hrs
Simulation, Advanced simulation, Signal Integrity			05 Hrs
PCB layout- Floor planning, component pre planning, PCB printing- 2 layer			05 Hrs
Functionality and performance check, Failure analysis, Validation and system integration			05 Hrs
System Analysis			05 Hrs

References

1. A. S Sedra and KC Smith, Microelectronic circuits, Oxford, 1998.
2. G.L. Ginsberg, Printed Circuit Design, McGraw Hill, 1991.

Program: Digital Electronics			
Course Title: Automotive Electronics		**Course Code:** 17EVEC708	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 5**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 40	**Examination Duration: 3 hrs**		
Chapter No. 1. Automotive Fundamentals Overview Introduction to Automotive Industry and Modern Automotive Systems Vehicle classifications and specifications need for electronics in automobiles, Application areas of electronics in the automobiles Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Spark pulse generation, Ignition Timing, Drive Train, Transmission, Brakes, Steering System.			8Hrs
Chapter No. 2. Sensors and Actuators Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor Strain gauge, Engine Coolant Temperature (ECT) Sensor, Knock Sensor, Throttle angle sensor, Fuel Injector Actuator, Ignition Actuator			7Hrs
Chapter No. 3. Electronic Engine Control Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle sped control, EGR Control			5Hrs
Chapter No. 4. Vehicle Motion Control and Safety Systems Cruise Control, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronic Stability Program.			6Hrs
Chapter No:5. Automotive communication protocols			3Hrs

Overview of Automotive communication protocols : CAN, LIN . **Chapter No. 6. Advanced Driver Assistance Systems (ADAS)** Lane Departure Warning, Collision Warning, Automatic Cruise Control, Pedestrian Protection, Headlights Control, Connected Cars technology and trends towards Autonomous vehicles. **Chapter No. 7. Automotive safety standards ISO26262 and Diagnostics** Functional Safety: Need for safety standard-ISO 26262, safety concept, safety process for product life cycle, safety by design, validation. Fundamentals of Diagnostics: Basic wiring system and Multiplex wiring system, Preliminary checks and adjustments, Self-diagnostic system. Fault finding and corrective measures, OBD & off board diagnostic.	5Hrs 6Hrs

Text books:

1. Denton.T – Automobile Electrical and Electronic Systems, Edward Arnold publication, 1995.

References:

1. William T.M – Automotive Electronic Systems, Heiemann Ltd., London ,1978.
2. Nicholas Navet – Automotive Embedded System Handbook, CRC Press, 2009.
3. BOSCH Automotive Handbook, Wiley Publications, 8th Edition, 2011.
4. Co-Verification of hardware & software for ARM SoC Design – Jason.R.Andrews, Newnes Publications, 2004.
5. Hardware Software co-design of embedded systems, F.Balarin, Kluwer Academic Oublishers, 1987.

Lab:

1. Demonstration of cut section modules: Engine, Transmission , Steering, Braking, Suspension - Automobile dept.
2. Electronic engine control system: Injection and Ignition control system Transmission trainer modules
3. Modeling an engine Vehicle model simulation with Simulink using PI CONTROLLER
4. Basic gate logic simulation and modeling using Simulink and realization on the hardware platform.
5. Seat belt warning system simulation and modeling using Simulink and realization on the hardware platform. Vehicle speed control based on the gear input simulation and modeling using Simulink and realization on the hardware platform.
6. Throttle control modeling and simulation using Simulink and realization on the hardware platform.
7. Accelerator pedal interfacing software modeling and simulation using Simulink and realization on the hardware platform.
8. Develop matlab code for stepper motor control and convert it to Simulink model and port it to embedded hardware

Program: II Semester Master of Technology (VLSI Design & Embedded Systems)			**Teaching Hours**
Course Title: Real Time Embedded System		**Course Code: 17EVEC709**	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 3 Hrs/week**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 45 Hrs	**Examination Duration:**		
UNIT I			

1. Building blocks: Real Time System, Types, Real Time Computing, Design Issue, Sample Systems, Hardware Requirements- Processor in a system, System Memories, System I/O, De-bouncing, Other Hardware Devices (A/D, D/A, USART, Watchdog Timers, Interrupt Controllers). Device Drivers, Interrupt Servicing Mechanism & Interrupt Latency.	**12 Hrs**
2. Advanced Processors: Automotive Grade Processors: AEC-Q100 qualification, Qorivva 32-bit Microcontrollers, MPC577XK for ADAS, AURIX from Infineon, Tricore Architecture, Renasas RL78/D1x (Automotive Only)	**10 Hrs**
UNIT II	
3. Real Time Operating System: Interrupt driven systems, foreground/background systems, full featured rtos, POSIX, buffering data, mailboxes, critical regions, semaphores, event flags & signals, deadlock, process stack management, dynamic allocation.	**04 Hrs**
4. Case Studies: Mucos/ VX Works Functions – System level, task service, time delay, memory allocation, semaphore, mailbox, queue. Example systems: Coding for Automatic chocolate vending machine using MUCOS & Coding for sending application layer byte streams on a TCP/IP Network using Vx Works.	**06 Hrs**
UNIT III	
5. Process of Embedded System Development: Development process, requirements engineering, design, implementation, integration & testing, packaging, configuration management, managing embedded system development, embedded system fiascos.	**08 Hrs**
6. Current trends, ethical & environmental issues The students shall give seminars on current trends in the field of RTES, ethical, & environmental issues.	**05 Hrs**

Text Books

1. Philip. A. Laplante, “Real-Time Systems Design and Analysis- an Engineer’s Handbook”- Second Edition, PHI Publications.
2. Rajkamal, “Embedded Systems: Architecture, Programming and Design”, Tata McGraw Hill, New Delhi, 2003.
3. Dr. K.V.K K Prasad, “Embedded Real Time Systems: Concepts Design and Programming”, Dreamtech Press New Delhi, 2003.

References

1. Joseph Yiu, “The Definitive guide to ARM CORTEX –M3 & CORTEX-M4 Processors”, Elsevier, Newnes, 2014.
2. Steve Furber “ARM System –on – Chip Architecture” Second Edition, Pearson Education
3. David E. Simon, “An Embedded software primer”, Pearson Education, 1999..
4. David A. Evesham, “Developing real time systems – A practical introduction”, Galgotia Publications, 1990
5. William Hohl, “ARM Assembly Language Fundamentals & Techniques”, CRC Press
6. C. M. Krishna, “Real Time Systems” MGH, 1997
7. Jane W.S. Liu, “Real-Time Systems”, Pearson Education Inc., 2000

Course Code: 17EVEC710	Course Title: **Advanced Digital Logic Design**
L-T-P: 1-0-3	Credits: 4
ISA Marks: 50+100	ESA Marks: 50
Teaching Hrs: 40	

Chapter No. 1. Digital Integrated Circuits Moore's law, Technology Scaling, Die size growth, Frequency, Power dissipation, Challenges in digital design, Design metrics, Cost of Integrated circuits, ASIC , Evolution of SoC ASIC Flow Vs SoC Flow, SoC Design Challenges. Introduction to CMOS Technology, PMOS & NMOS Operation, CMOS Operation principles, Characteristic curves of CMOS, CMOS Inverter and characteristic curves, Delays in inverters, Buffer Design, Power dissipation in CMOS, CMOS Logic, Stick diagrams and Layout diagrams. Setup time, Hold Time, Timing Concepts.	10 hrs
Chapter No. 2. Digital Building Blocks Basic Gates, Universal Gates, nand & nor Implementations. Decoder, encoder, code converters, Priority encoder, multiplexer, demultiplexer, Comparators, Parity check schemes, Multiplexer, De-multiplexer, Pass Transistor Logic, application of multiplexer as a multi-purpose logical element. Asynchronous and synchronous up-down counters, Shift registers. FSM Design, Mealy and Moore Modelling, Adder & Multiplier concepts, Memory Concept	10 hrs
Chapter No. 3. Logic Design Using Verilog Evolution & importance of HDL, Introduction to Verilog, Levels of Abstraction, Typical Design Flow, Lexical Conventions, Data Types Modules, Nets, Values, Data Types, Comments, arrays in Verilog, Expressions, Operators, Operands, Arrays, memories, Strings , Delays , parameterized designs Procedural blocks, Blocking and Non-Blocking Assignment, looping, flow Control, Task, Function, Synchronization, Event Simulation. Need for Verification, Basic test bench generation and Simulation	12 hrs
Chapter No. 4. Principles of RTL Design Verilog Coding Concepts, Verilog coding guide lines: Combinational, Sequential, FSM. General Guidelines, Synthesizable Verilog Constructs, Sensitivity List, Verilog Events, RTL Design Challenges, Clock Domain Crossing. Verilog modelling of combinational logic and sequential logic	8 hrs
Chapter No. 5. Design and simulation of Architectural building blocks Basic Building blocks design using Verilog HDL: Arithmetic Components – Adder, Subtractor, and Multiplier design, Data Integrity – Parity Generation circuits, Control logic – Arbitration, FSM Design – overlapping and non-overlapping Mealy and Moore state machine design	10 hrs

Reference Books:

1. Digital Design by Morris Mano M, 4th Edition
2. Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, 2nd Edition
3. Principles of VLSI RTL Design: A Practical Guide by Sapan Garg, 2011 Tools: 1. NC Verilog, NC Sim, CVER + GTKWave, VCSMX, Modelsim for Verilog 2. Microwind for layout.

Course Code: 17EVEC711	**Course Title: Testing & IC Characterization**	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hrs: 5 hrs/week**
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**
Teaching Hrs: 40		**Exam Duration: 03 hrs**

Content	**Hrs**
CHAPTER NO. 1. VERIFICATION CONCEPTS Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.	10 hrs
CHAPTER NO. 2. SYSTEM VERILOG – LANGUAGE CONSTRUCTS System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.	10 hrs
CHAPTER NO. 3. SYSTEM VERILOG – CLASSES & RANDOMIZATION SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism. Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization.	12 hrs
CHAPTER NO. 4. SYSTEM VERILOG – ASSERTIONS & COVERAGE Assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Coverage driven verification : Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.	8 hrs
CHAPTER NO. 5. BUILDING TESTBENCH LAYERED TESTBENCH ARCHITECTURE. INTRODUCTION TO UNIVERSAL VERIFICATION METHODOLOGY, OVERVIEW OF UVM BASE CLASSES AND SIMULATION PHASES IN UVM AND UVM MACROS. UNIFIED MESSAGING IN UVM, UVM ENVIRONMENT STRUCTURE, CONNECTING DUT- VIRTUAL INTERFACE	10 hrs
REFERENCES: 1. SYSTEM VERILOG LRM 2. CHRIS SPEAR, GREGORY J TUMBUSH - SYSTEMVERILOG FOR VERIFICATION - A GUIDE TO LEARNING THE TESTBENCH LANGUAGE FEATURES - SPRINGER, 2012 3. STEP-BY-STEP FUNCTIONAL VERIFICATION WITH SYSTEMVERILOG AND OVM BY SASAN IMAN SIMANTIS INC. SANTA CLARA, CA SPRING 2008 TOOLS: 1. NC VERILOG, NC SIM, VCSMX FOR SYSTEM.	

Course Code: 17EVEE703	Course Title: **Standard Cell Design and Layout**	
L-T-P: 2-0-1	Credits: 3	Contact Hrs:
ISA Marks: 50+100	ESA Marks: 50	Total Marks: 200
Teaching Hrs: 50		Exam Duration: 3 hrs

Chapter No. 1. Introduction IC design flows. Use of standard cell elements vs. custom design and Gate array paradigms. Introduction to memory types and construction of memory elements.	15 hrs
Chapter No. 2. Standard cell library composition and usage Types of standard cell elements. Logical and functional elements, primitives and complex macros. Sequential elements and register files. (Flip flop and latch design). Data path elements. Library size vs. usage in standard flows. Drive strength and cell families. Layout of library elements – single height, double height cells. Power Management cells.	17hrs
Chapter No. 3. Standard cell characterization Usage of standard cells by various tools. Information needed at each stage of design flow. Characterization parameters, setup and runs across PVT corners. Library representation formats. (Gate level simulation, synthesis, timing, layout, timing, LVS, DRC)	18 hrs
References: Standard cell and memory library documentation by Vendors 90nm EDK library	

Program: VLSI Design & Embedded Systems			
Course Title: Low Power VLSI Circuits		**Course Code:** 17EVEE704	
L-T-P: 2-0-1	**Credits: 4**	**Contact Hours:4**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 40	**Examination Duration: 3 hours**		
1: Introduction to low power VLSI design: Need for Low Power VLSI Chips, sources of power dissipation. Device and Technology impact on Low Power, dynamic power dissipation in CMOS. Power Estimation.			6Hrs
2: Power analysis: Simulation Power Analysis, Spice circuits simulator, gate level logic simulator, Probabilistic power analysis			5Hrs
3: A new CMOS driver model for transient analysis and power dissipation analysis, low power design of off-chip drivers and transmission lines: a branch and bound approach.			5Hrs
4: Different levels of power optimization Low Power Design; circuit Level, logic Level, Low Power Architecture.			7Hrs
5: Floor plan design with low power considerations, optimal drivers of high-speed low power ics, retiming sequential circuits for low power			5Hrs
6: Clock Distribution: Low Power Clock distribution, single driver versus distributed buffers. Power management: Power & performance management,switching activity reduction, parallel architecture.			4Hrs
7:Algorithmic level methodologies for power reduction: Algorithm and architectural level methodologies- algorithmic level analysis & optimization, architecture level estimation and synthesis, Current trends			8Hrs
Text Books			

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002.
2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997.

Reference Books:

1. A. Chandrakasan and R. Brodersen, “Low Power CMOS Design”.
2. Sung - Mo Kang & Yosuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, TMH, 2003 (Third Edition).
3. Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, “System-on-chip Test Architectures”, 2008.
4. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000.

Program: VLSI Design & Embedded Systems		
Course Title: Analog and Mixed mode VLSI Circuits		**Course Code: 17EVEE705**
L-T-P: 2-0-1	**Credits: 3**	**Contact Hours: 6**
ISA Marks: 50	**ESA Marks: 50**	
Teaching Hours: 50	**Examination Duration: 3 hours**	**Total Marks: 100**

1. Introduction to CMOS analog circuits, MOS transistor DC and AC small signal parameters from large signal model, Common source amplifier with resistive load, diode load and current source load, Source follower, Common gate amplifier, Cascode amplifier, Frequency response of amplifiers.	12 hrs
2. Current source/sink/mirror, Matching, Wilson current source, Widlar current source and Regulated Cascode current source, Differential amplifier.	08 hrs
3. Op-Amp: CMOS Op-Amp, Compensation of Op-Amp,Design of two stage Op-Amp.	06 hrs
4. Basic Current reference, and Voltage (Bandgap) reference circuits, OPAMP based references, Current mode bandgap reference.	06 hrs
5. Bidirectional analog switch, Sample and Hold circuit, Basic Comparator architecture, non-idealities (offset error, bandwidth consideration), Dynamic comparator, Sense amplifier, Current Mode Logic(Buffer and Latch)	08 hrs
6. Data Converter Fundamentals, DAC architectures and ADC architectures	10 hrs

Text Books

1. Phillip. E. Allen, Douglas R. Holberg, “CMOS Analog circuit Design” Oxford University Press, 2002.
2. Baker, Li, Boyce, “CMOS: Circuit Design, Layout and Simulation”, Prentice Hall of India, 2000

Reference Books

1. N. Weste and K. Eshranghian, Principles of CMOS VLSI Design, Addison Wesley. 1985.
2. J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997
3. B Razavi ‘Design of Analog CMOS Integrated Circuits’ First Edition McGraw Hill 2001

Lab:

1. Design and implement Common source MOS amplifier with resistive load, diode load and current source load.
2. Design and implement a Cascode amplifier.
3. Design and implement a Simple current mirror
4. Design and implement a Differential amplifier
5. Design and implement a Operational amplifier
6. Design and implement a basic comparator
7. Design and implement a R-2R DAC

Program: III Semester Master of Technology (VLSI Design & Embedded Systems)			**Teaching Hours**
Course Title: Embedded Software Design		**Course Code: 17EVEC801**	
L-T-P: 0-0-3	**Credits: 3**	**Contact Hours: 6 Hrs/week**	
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**	
Teaching Hours: 40 Hrs	**Examination Duration:**		
1. Introduction To Real-Time Operating Systems: Introduction to OS, Introduction to real time embedded system- real time systems, characteristics of real time systems, and the future of embedded systems. Introduction to RTOS, key characteristics of RTOS, its kernel, components in RTOS kernel, objects, scheduler, services, context switch, Scheduling types: Preemptive priority-based scheduling, Round-robin and preemptive scheduling.			**08 Hrs**
2. Tasks, Semaphores and Message Queues:: A task, its structure, A typical finite state machine, Steps showing the how FSM works. A semaphore, its structure, binary semaphore, mutual exclusion (mutex) semaphore, Synchronization between two tasks and multiple tasks, Single shared-resource-access synchronization, Recursive shared-resource-access synchronization. A message queue, its structure, Message copying and memory use for sending and receiving messages, Sending messages in FIFO or LIFO order, broadcasting messages.			**08 Hrs**
3. Typical RTOSs: Study of VX works, RT Linux and Android OS and comparisons. Real time programming using RTX/free RTOS. Applications and Common Design Problems: Embedded RTOS for Image Processing & Control Systems, and common problems encountered in these applications.			**04 Hrs**
4. Introduction to embedded linux: Embedded Linux overview: Development-Kernel architectures and device driver model-Embedded development issues-Tool chains in Embedded Linux-GNU Tool Chain (GCC,GDB, MAKE, GPROF & GCONV)- Linux Boot process			**02 Hrs**
5. Boot sequence-System loading, sys linux, Lilo, grub-Root file system-Binaries required for system operation-Shared and static Libraries overview-Writing applications in user space-GUI environments for embedded Linux system			**02 Hrs**
6. File system in Linux: File system Hierarchy-File system Navigation -Managing the File system –Extended file systems-INODE-Group Descriptor-Directories-Virtual File systems-Performing File system Maintenance - Locating Files –Registering the File systems-Mounting and Un-mounting –Buffer cache-/proc file systems-Device special files			**08 Hrs**
7. Program design and Analysis : Components of Embedded system: State machines; stream oriented programming and circular buffers, queues. Models of programs: data flow graph and control flow graphs, Assembly, linking and loading. Basic compilation techniques: Statement translation, procedures, data structures. Program optimization: Expression simplification, dead code elimination, procedure inlining, loop transformations, register allocation, scheduling, instruction selection, interpreters and JIT compilers. Program level performance analysis, software performance optimization, program level energy and power analysis, analysis and optimization of program size. Program validation and testing: Clear box testing, black box testing, evaluating function tests.			**08 Hrs**

Text Books

1. Qing Li with Caroline Yao, “Real-Time Concepts for Embedded Systems”, Published by CMP Books,2011
2. Dr. K.V.K.K. Prasad, “Embedded/Real-time systems: concepts, Design & Programming”, published by dreamtech press .
3. “Embedded Systems- Architecture, Programming and Design” by Raj Kamal, TMH

References

1. Philip.A.Laplante, “Real Time System Design and Analysis”, Prentice Hall of India, 3rd Edition, April 2004.
2. “Programming embedded systems” in C and C++ Micheal Barr orielly

List of Experiments:

1. Write a ‘C’ program & demonstrate concept of Task Scheduling.
2. Write a ‘C’ program & demonstrate concept of Semaphore.
3. Write a ‘C’ program & demonstrate concept of Mailbox.
4. Write a ‘C’ program & demonstrate concept of S/W Interrupts.
5. Write a ‘C’ program & demonstrate concept of interrupts.
6. Write a ‘C’ program & demonstrate concept of Inter Task Communication.

Reference Books

1. Dr. K.V.K.K. Prasad, “Embedded/Real-time systems: concepts, Design & Programming”, published by dreamtech press.

Manual

1. LPC2148 datasheet by NXP.

LPC2148 board manual by ALS, Bangalore.

Course Code: 17EVEC802	Course Title: **Advanced Digital logic Verification**	
L-T-P: 1-0-3	Credits: 4	Contact Hrs: 6hrs/week
ISA Marks: 50+100	ESA Marks: 50	Total Marks: 200
Teaching Hrs: 50		Exam Duration: 3 hrs

Chapter No. 1. Verification Concepts Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.	10 hrs
Chapter No. 2. System Verilog – Language Constructs System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.	10 hrs
Chapter No. 3. System Verilog – Classes & Randomization SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism. Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization.	12 hrs
Chapter No. 4. System Verilog – Assertions & Coverage Assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Coverage driven verification : Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.	8 hrs
Chapter No. 5. Building Testbench Layered testbench architecture. Introduction to Universal Verification Methodology, Overview of UVM	10 hrs

Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface	
References: 1. System Verilog LRM 2. Chris Spear, Gregory J Tumbush - SystemVerilog for verification - a guide to learning the testbench language features - Springer, 2012 **3.** Step-by-Step Functional Verification with SystemVerilog and OVM by Sasan Iman SiMantis Inc. Santa Clara, CA Spring 2008 Tools: 1. NC Verilog, NC Sim, VCSMX for System.	

Program: III Semester Master of Technology (VLSI Design & Embedded Systems)			**Teaching Hours**
Course Title: Internet of Things		**Course Code: 17EVEE801**	
L-T-P: 2-0-1	**Credits: 3**	**Contact Hours: 5 Hrs/week**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 25 Hrs	**Examination Duration:**		

1	**Introduction to Internet of Things (IoT)** Definition & Characteristics of IoT, Things in IoT, IoT protocols, IoT functional blocks, communication models and APIs.	**04 hrs**
2	**IoT Architecture** Enabling technologies: Sensors, Zigbee, Bluetooth, IoT ecosystem, Data Link protocols: IEEE 802.15.4e, IEEE 802.11.ah, DASH7, Low Power Wide Area Network (LoRaWAN).	**04 hrs**
3	**Network protocols** Routing Protocol for Low-Power and Lossy Networks (RPL), cognitive RPL (CORPL), Channel-Aware Routing Protocol (CARP), Low power Wireless Personal Area Networks (LoWPAN).	**04 hrs**
4	**Application and Security protocols** Message Queue Telemetry Transport (MQTT), MQTT for Sensor Networks, Secure MQTT, Advanced Message Queuing Protocol (AMQP), Constrained Application Protocol (CoAP), OPC UA, 6LoWPAN), Routing Protocol for Low-Power and Lossy Networks (RPL).	**04 hrs**
5	**IoT Platforms Design Methodology** IoT Design Methodology, Case Study on IoT System for Weather Monitoring etc., Basic building blocks of an IoT device, Raspberry Pi, interface (serial, SPI, I2C), IoT Operating Systems: Contiki, RIOT.	**04 hrs**
6	**Programming with Raspberry Pi** XML, JSON, SOAP and REST-based approach, WebSocket protocol.	**04 hrs**
7	**IoT prototyping** Business models, example applications: Case studies on Home automation, Cities, Environment, Energy, Agriculture, Health with emphasis on data analytics and security.	**06 hrs**

Text Books:

1. Arshdeep Bahga, Vijay Madisetti “Internet of Things (A Hands-on-Approach)” Universities Press- 2014.
2. Olivier Hersent, David Boswarthick, Omar Elloumi, “The Internet of Things: Key Applications and Protocols”

John Wiley & Sons – 2012.

Reference Books:

1. Subhas Chandra Mukhopadhyay “Internet of Things Challenges and Opportunities” Springer- 2014.

Lab:

1. Programming with Raspberry Pi
2. Cloud service interface for data storage and retrieval
3. Performance analysis of Data link protocols, routing and application protocols
4. Open Ended Experiment with focus on data analytics and security

Course Code: 17EVEE802	Course Title: AUTOSAR	
L-T-P : 2-0-1	Credits: 3	Contact Hrs: 3 Hours
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3

Content	Hrs
Unit - 1	
Chapter No. 1: AUTOSAR Fundamentals Evolution of AUTOSAR – Motivations and Objectives AUTOSAR consortium – Stake holders – work Packages, AUTOSAR Partnership, Goals of the partnership, Organization of the partnership, AUTOSAR specification, AUTOSAR Current development status, BSW Conformance classes: ICC1, ICC2, ICC3, and Drawbacks of AUTOSAR.	8 hrs
Chapter No. 2: AUTOSAR layered Architecture AUTOSAR Basic software, Details on the various layers , Details on the stacks Virtual Function Bus (VFB) Concept Overview of AUTOSAR Methodology , Tools and Technologies for AUTOSAR AUTOSAR Application Software Component (SW-C) ,Types of SW-components AUTOSAR Run Time Environment (RTE): RTE Generation Process: Contract Phase, Generation Phase, MCAL, IO HW Abstraction Layer, Partial Networking, Multicore, J1939 Overview, AUTOSAR Ethernet, AUTOSAR E2E Overview , AUTOSAR XCP, Metamodel , From the model to the process , Software development process.	7 hrs
Unit - 2	
Chapter No. 3: Methodology of AUTOSAR and Communication in AUTOSAR CAN Communication, CAN FD, CAN in Automation, CANape, Application Layer and RTE, intra and inter ECU communication, Client-Server Communication, Sender-Receiver, Communication, CAN Driver, Communication Manager (ComM), Overview of Diagnostics Event and Communication Manager	10 hrs
Chapter No. 4: BSW Development and Integration BSW Constituents: Memory layer, COM and Services layer, ECU abstraction, AUTOSAR, Operating system, Interfaces: Standard interface, AUTOSAR standardized interface, BSW-RTE interface,(AUTOSAR interface), BSW-ECU hardware interface, Complex device drivers and BSW module configuration, AUTOSAR Integration.	5 hrs
Unit - 3	
Chapter No. Chapter 5: Infotainment Systems in Automobiles Infotainment Systems Fundamentals: Radio, Multimedia, and Navigation: Introduction to In Vehicle Infotainment (IVI) systems, Use of operating systems in IVI , GENIVI Alliance, Tuner: AM/FM, XM/Sirrus, DAB/DMB, Software Defined Radio; Concepts of HD, radio, Ensemble, Traffic Announcements, Spread Spectrum, d. Multimedia: Types of Media; Music, Video, Podcasts, etc.	5 hrs

Media management; Playback, Track Control, Metadata, Playlists, Categories, Trick play, Audio/Video Source Management, Navigation: Points of Interests, Routes, Waypoints, Dead Reckoning position, Traffic Info, GLONASS, GNSS, RTK, GPS, and SBAS/GBAS,INS f. Media types: CD, DVD, CDDA, USB, SDCARD, Media Formats:MP3, WMV, RealAudio/Video, QTP, Architecture – Design Patterns - Proxies, Adaptors, Interfaces, Singleton, Factory method	
Chapter No. Chapter 6: Communication Systems in Automobiles Automotive & Consumer Electronic Communication Systems: Introduction to Bluetooth – Pairing, HFP, A2DP, PAN, PBAP, DUN, Concepts of MOST network, DLNA, AVB, Concepts of TCP/IP, Ethernet, WiFi, WiFi Direct, MyWiFi and CAN, Mirror link, Tethering	5 hrs
Text Book (List of books as mentioned in the approved syllabus) 1. Ribbens, Understanding of Automotive electronics, 6th Edition, Elsevier, 2003 2. Denton.T, Automobile Electrical and Electronic Systems, Elsevier, 3rd Edition, 2004 3. Denton.T, Advanced automotive fault diagnosis, 2000 **References** 1. Ronald K Jurgen, Automotive Electronics Handbook, 2nd Edition, McGraw-Hill, 1999 2. James D Halderman, Automotive electricity and Electronics, PHI Publication, 2000 3. Allan Bonnick, Automotive Computer Controlled Systems Diagnostic Tools and Techniques, Elsevier Science, 2001 4. Nicholas Navet , Automotive Embedded System Handbook , 2009	

Course Code: 17EVEE803	Course Title: ASIC Design	
L-T-P: 2-0-1	Credits: 4	Contact Hrs: 50
ISA Marks: 50+100	ESA Marks: 50	Total Marks: 200
Teaching Hrs: 50		Exam Duration: 3 hrs

Content	**Hrs**
Chapter No. 1. Introduction to ASIC ASIC types, design flow, economics of ASIC	8 hrs
Chapter No. 2. ASIC design library and Logic cell Transistor as register, transistor parasitic capacitance, Logic Effort, Data Path Elements, Adders, Multiplier, Sequential logic cells, I/O cell.	10 hrs
Chapter No. 3. Logic Synthesis and Simulation Logic synthesis, FSM synthesis, structural simulation, static timing analysis, delay models	10 hrs
Chapter No. 4. ASIC Construction Floor planning and placement and routing Physical Design, System Partitioning, Estimating ASIC size, partitioning methods.	10 hrs
Chapter No. 5. Floor planning and placement and routing Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.	12 hrs
Text Books: 1. M.J.S .Smith, - “Application - Specific Integrated Circuits” – Pearson Education, 2003. 2. Randall L Geiger, Phillip E. Allen, “Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits”, McGraw Hill International Company, 1990.	

References:

1. Jose E.France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing”, Prentice Hall, 1994.
2. Andrew Brown, - “VLSI Circuits and Systems in Silicon”, McGraw Hill, 1991.
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, “Field Programmable Gate Arrays”- Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, “Analog VLSI Signal and Information Processing “, McGraw Hill, 1994.
5. S. Y. Kung, H. J. Whilo House, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.

Program: Digital Electronics			**Teaching Hours**
Course Title: Machine learning		**Course Code: 17EVEC705**	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 5 Hrs/week**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 40 Hrs	**Examination Duration: 3 hrs**		
Chapter No. 1: Introduction Introduction What is Machine Learning? Applications of Machine Learning, Types of Machine Learning: Supervised, Unsupervised and Reinforcement learning, Dataset formats, Basic terminologies.			**05 Hrs**
Chapter No. 2: Supervised Learning Linear Regression, Logistic Regression Linear Regression: Single and Multiple variables, Sum of squares error function, The Gradient descent algorithm, Application, Logistic Regression, The cost function, Classification using logistic regression, one-vs-all classification using logistic regression, Regularization.			**10 Hrs**
Chapter No. 3: Supervised Learning: Neural Network Introduction to perception learning, Implementing simple gates XOR, AND, OR using neural network. Model representation, Gradient checking, Back propagation algorithm, Multi-class classification, Application- classifying digits, SVM.			**10 Hrs**
Chapter No. 4: Unsupervised Learning: Clustering Introduction, K means Clustering, Algorithm, Cost function, Application.			**05Hrs**
Chapter No. 5: Unsupervised Learning: Dimensionality reduction Dimensionality reduction, PCA- Principal Component Analysis. Applications, Clustering data and PCA.			**05Hrs**
Chapter No. 6: Machine Learning System Design Evaluating a hypothesis, Model selection, Bias and variance, error analysis, error metrics for skewed classes. Building a Model.			**05 Hrs**

Text Book (List of books as mentioned in the approved syllabus)

1. Tom Mitchell, Machine Learning, 1, McGraw-Hill. , 1997
2. Christopher Bishop, Pattern Recognition and Machine Learning, 1, Springer, 2007

References

1. Video lectures by : Andrew Ng, Co-founder, Coursera; Adjunct Professor, Stanford University; formerly head of Baidu AI Group/Google Brain https://www.coursera.org/learn/machine-learning#
2. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning : Data Mining, Inference and Prediction, 2, Springer, 2009

Implementation Assignments:

1. Assignments are designed to explore the concepts like
   - Supervise and unsupervised learning,
   - Clustering,
   - Regression and estimation
2. Motivate students to take up open challenges like Kaggle, walmart, ect
3. To explore different Machine Learning Tools/ Libraries.

Program: Digital Electronics		
Course Title: Advanced Computer Architecture		**Course Code:** 17EVEC801
L-T-P-SS: 4-0-0	**Credits: 4**	**Contact Hours: 4**
CIE Marks: 50	**SEE Marks: 50**	**Self Study : --**
Teaching Hours: 50	**Examination Duration: 3 hours**	**Total Marks: 100**

1. Parallel Computers Models: Introduction. State of Computing and classification of parallel Computers, Multiprocessors and multi computers. Multivector and SIMD Computers.	7 hrs
2. Program properties: Conditions of Parallelism Data & resource Dependences, H/W & S/W parallelism, Program partitioning, Scheduling Grain size & latency, program flow Mechanisms.	6 hrs
3. System Interconnect Architecture: Network Properties and routing, Static & dynamic interconnection networks, Multiprocessor system interconnects, Hierarchical bus systems, Crossbar switch, Multipart memory, Multistage & combining network.	5 hrs
4. Advanced processors : Advanced processor technology, instruction-set architectures, CISC scalar processors, RISC scalar processors, Superscalar processors, VLIW architectures, VLIW architectures.	6 hrs
5. Pipelining: Linear pipeline processor, Nonlinear pipeline processor, Instruction pipeline design, Branch handling techniques, Arithmetic pipeline design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipeline	8 hrs
6. Memory Hierarchy Design: Cache basics, Miss rate and penalty, Cache Hierarchy, Memory Organizations, Memory Hierarchy	6 hrs
7. Multiprocessor Architecture and Programming: Symmetric shared memory architectures, Distributed shared memory architectures, Models of memory consistency, Cache coherence protocols (MSI, MESI and MOESI), Scalable cache coherence	6 hrs
8. Scalable & multithreaded architecture : Latency Hiding Techniques, Principles of multithreading, Scalable multithreadeded architectures	2 hrs
9. Introduction to Intel architectures Intel core Duo processor, CPU, Memory controller, I/O Controller	4 hrs

Text Books

1. Kai Hwang, Faye A. Briggs, “Computers Architecture and Parallel Processing” MGH – 1985
2. Kai Hwang, “ Advanced Computer Architecture – TMH – 1993
3. D. Sima,T. Fountain, P.Kasuk,” Advanced Computer Architecture-A Design Space Approach” Addisson Wesley,1997.
4. M. J. Flynn,”Computer Architecture, Pipelined And Parallel Processing”, Narosa Publications,1998

Reference Books:

1. Neil D. A. Patterson and J. L. Hennessey “Computer Organization and Design”, Morgan , Kaufmann,2002

2. Stalling W. "Computer Organization and Architecture- Designing for performance" ,PHI,2005.
3. D.E. Culler and J.P.Singh " Parallel Computer Architechure", Harcourt Asia PTE Ltd,2000

Program: VLSI Design & Embedded Systems			
Course Title: Automotive Electronics		**Course Code:** 19EVEC701	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 5**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 40	**Examination Duration: 3 hrs**		

Chapter No. 1. Automotive Fundamentals Overview Introduction to Automotive Industry and Modern Automotive Systems Vehicle classifications and specifications need for electronics in automobiles, Application areas of electronics in the automobiles Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Spark pulse generation, Ignition Timing, Drive Train, Transmission, Brakes, Steering System.	8Hrs 7Hrs
Chapter No. 2. Sensors and Actuators Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor Strain gauge, Engine Coolant Temperature (ECT) Sensor, Knock Sensor, Throttle angle sensor, Fuel Injector Actuator, Ignition Actuator	
Chapter No. 3. Electronic Engine Control Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle sped control, EGR Control	5Hrs
Chapter No. 4. Vehicle Motion Control and Safety Systems Cruise Control, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronic Stability Program.	6Hrs
Chapter No:5. Automotive communication protocols Overview of Automotive communication protocols : CAN, LIN .	3Hrs
Chapter No. 6. Advanced Driver Assistance Systems (ADAS) Lane Departure Warning, Collision Warning, Automatic Cruise Control, Pedestrian Protection, Headlights Control, Connected Cars technology and trends towards Autonomous vehicles.	5Hrs
Chapter No. 7. Automotive safety standards ISO26262 and Diagnostics Functional Safety: Need for safety standard-ISO 26262, safety concept, safety process for product life cycle, safety by design, validation. Fundamentals of Diagnostics: Basic wiring system and Multiplex wiring system, Preliminary checks and adjustments, Self-diagnostic system. Fault finding and corrective measures, OBD & off board diagnostic.	6Hrs

Text books:

2. Denton.T – Automobile Electrical and Electronic Systems, Edward Arnold publication, 1995.

References:

6. William T.M – Automotive Electronic Systems, Heiemann Ltd., London ,1978.
7. Nicholas Navet – Automotive Embedded System Handbook, CRC Press, 2009.
8. BOSCH Automotive Handbook, Wiley Publications, 8th Edition, 2011.
9. Co-Verification of hardware & software for ARM SoC Design – Jason.R.Andrews, Newnes Publications, 2004.
10. Hardware Software co-design of embedded systems, F.Balarin, Kluwer Academic Oublishers,

1987.

Lab:

9. Demonstration of cut section modules: Engine, Transmission , Steering, Braking, Suspension - Automobile dept.
10. Electronic engine control system: Injection and Ignition control system Transmission trainer modules
11. Modeling an engine Vehicle model simulation with Simulink using PI CONTROLLER
12. Basic gate logic simulation and modeling using Simulink and realization on the hardware platform.
13. Seat belt warning system simulation and modeling using Simulink and realization on the hardware platform. Vehicle speed control based on the gear input simulation and modeling using Simulink and realization on the hardware platform.
14. Throttle control modeling and simulation using Simulink and realization on the hardware platform.
15. Accelerator pedal interfacing software modeling and simulation using Simulink and realization on the hardware platform.
16. Develop matlab code for stepper motor control and convert it to Simulink model and port it to embedded hardware

Program: VLSI Design & Embedded Systems			
Course Title: AUTOSAR and Infotainment		Course Code: **19EVEE707**	
L-T-P : 2-0-1	Credits: 3	Contact Hrs: 4	
CIA Marks: 50	SEE Marks: 50	Total Marks: 100	
Teaching Hrs: 24	Exam Duration: 3 hrs		
Chapter No. 1: AUTOSAR Fundamentals Evolution of AUTOSAR – Motivations and Objectives AUTOSAR consortium – Stake holders – work Packages, AUTOSAR Partnership, Goals of the partnership, Organization of the partnership, AUTOSAR specification, AUTOSAR Current development status, BSW Conformance classes: ICC1, ICC2, ICC3, and Drawbacks of AUTOSAR.			4 hrs
Chapter No. 2: AUTOSAR layered Architecture AUTOSAR Basic software, Details on the various layers , Details on the stacks Virtual Function Bus (VFB) Concept Overview of AUTOSAR Methodology , Tools and Technologies for AUTOSAR AUTOSAR Application Software Component (SW-C) ,Types of SW-components AUTOSAR Run Time Environment (RTE): RTE Generation Process: Contract Phase, Generation Phase, MCAL, IO HW Abstraction Layer, Partial Networking, Multicore, J1939 Overview, AUTOSAR Ethernet, AUTOSAR E2E Overview , AUTOSAR XCP, Metamodel , From the model to the process , Software development process.			4 hrs
Unit - 2			
Chapter No. 3: Methodology of AUTOSAR and Communication in AUTOSAR CAN Communication, Application Layer and RTE, intra and inter ECU communication, Client-Server Communication, Sender-Receiver, Communication, CAN Driver, Communication Manager (ComM), Overview of Diagnostics Event and Communication Manager			4 hrs
Chapter No. 4: BSW Development and Integration BSW Constituents: Memory layer, COM and Services layer, ECU abstraction, AUTOSAR, Operating system, Interfaces: Standard interface, AUTOSAR standardized interface, BSW-RTE interface,(AUTOSAR interface), BSW-ECU hardware interface, Complex device drivers and BSW module configuration, AUTOSAR Integration.			4 hrs
Chapter No. Chapter 5: Infotainment Systems in Automobiles			4 hrs

Infotainment Systems Fundamentals: Radio, Multimedia, and Navigation: Introduction to In Vehicle Infotainment (IVI) systems, Use of operating systems in IVI , GENIVI Alliance, Tuner: AM/FM, XM/Sirrus, DAB/DMB, Software Defined Radio; Concepts of HD, radio, Ensemble, Traffic Announcements, Spread Spectrum, d. Multimedia: Types of Media; Music, Video, Podcasts, etc. Media management; Playback, Track Control, Metadata, Playlists, Categories, Trick play, Audio/Video Source Management, Navigation: Points of Interests, Routes, Waypoints, Dead Reckoning position, Traffic Info, GLONASS, GNSS, RTK, GPS, and SBAS/GBAS,INS f. Media types: CD, DVD, CDDA, USB, SDCARD, Media Formats:MP3, WMV, RealAudio/Video, QTP, Architecture – Design Patterns - Proxies, Adaptors, Interfaces, Singleton, Factory method	
Chapter No. Chapter 6: Communication Systems in Automobiles Automotive & Consumer Electronic Communication Systems: Introduction to Bluetooth – Pairing, HFP, A2DP, PAN, PBAP, DUN, Concepts of MOST network, DLNA, AVB, Concepts of TCP/IP, Ethernet, WiFi, WiFi Direct, MyWiFi and CAN, Mirror link, Tethering	4 hrs
Text Books (List of books as mentioned in the approved syllabus) Ronald K. Jurgen, Infotainment systems, 2007, SAE International, 2007	