KLE Technological University Creating Value Leveraging Knowledge	School of Electronics & Communication Engineering **PG – Digital Electronics**

Course Title: Principles and Practices of Engineering Education		**Course Code:** 15ECRC701	
L-T-P: 2-0-1	**Credits: 3**	**Contact Hours: 3**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 40	**Examination Duration: 3 hrs**		
1. **Fundamental Principles of Teaching and Learning**			**8 Hours**
2. **Learning Styles and Theories**			**8 Hours**
3. **Instructional Design Models and Technology Enhanced Learning**			**8 Hours**
4. **Assessment and Evaluation**			**8 Hours**
5. **Engineering Learning Modules**			**8 Hours**

Program: Digital Electronics			
Course Title: Fault diagnoses and testing for VLSI circuits		**Course Code:** 15EDEC708	
L-T-P: 4-0-0	**Credits: 4**	**Contact Hours: 4**	
CIE Marks: 50	**SEE Marks: 50**	**Total Marks: 100**	
Teaching Hours: 50	**Examination Duration: 3 hours**		
1. Threshold Logic: Introduction, Synthesis of threshold networks.			5 hrs
2. Reliable Design And Fault Diagnosis: Different types of Faults, Fault Detection in Combinational Circuits, Fault Location Experiments, Different approaches used in fault diagnosis of Combinational Circuits, Failure Tolerant Design, Quadded Logic.			15 hrs
3. Capabilities, Minimization and Transformation of Sequential Machines: Finite State Model (FSM) used in Machine design, Capabilities & Limitations of finite state machines, State equivalence and machine minimization, Simplification of incompletely specified machines.			10hrs
4. Structure of Sequential Machines: State Assignments Using Partitions, The Lattice of Closed Partitions, Reduction of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of Closed Partitions by State Splitting, Information Flow in Sequential Machines, Machine Decomposition.			10 hrs
5. State-Identification And Fault-Detection Fault detection / location Experiments, Machine Identification, Fault-Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault-Detection Experiments, Fault-Detection Experiments for Machines, Which have no Distinguishing Sequences.			10 hrs
Text Books **1.** Khohavi ZVI Switching and Finite Automata Theory, 2ed., TMH, 1999,			
Reference Books: **2.** Samuel Lee Digital Circuits & Logic Design, PHI, 1990			

Program: Digital Electronics		
Course Title: Real Time Embedded System lab		**Course Code:** 15EDEP706
L-T-P: 0-0-1	**Credits: 1**	**Contact Hours: 2**
CIE Marks: 80	**SEE Marks: 20**	**Total Marks: 100**
Lab Hours: 20	**Examination Duration: 3 hours**	
Experiments		

I Advanced Embedded Systems

1. Use any EDA (Electronic Design Automation) tool to learn the Embedded Hardware Design and for PCB design.

2. Familiarize the different entities for the circuit diagram design.

3. Familiarize with the layout design tool, building blocks, component placement, routings, design rule checking etc.

II Embedded Programming Concepts (RTOS)

4. Create „n" number of child threads. Each thread prints the message " I"m in thread number …" and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.

5. Implement the multithread application satisfying the following :

i.Two child threads are crated with normal priority.

ii.Thread 1 receives and prints its priority and sleeps for 50ms and then quits.

iii.Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits.

iv The main thread waits for the child thread to complete its job and quits.

6. Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.

7. Test the program below using multithread application-

i.The main thread creates a child thread with default stack size and name Child_Thread".

ii. The main thread sends user defined messages and the message „WM_QUIT" randomly to the child thread.

iii. The child thread processes the message posted by the main thread and quits when it receives the „WM_QUIT" message.

iv. The main thread checks the termination of the child thread and quits when the child thread complete its execution.

v. The main thread continues sending the random messages to the child thread till the „WM_QUIT" message is sent to child thread.

vi. The messaging mechanism between the main thread and child thread is synchronous.

Program: Digital Electronics			
Course Title: Data Structure using C		**Course Code:** 17EDEC701	
L-T-P: 0-0-1	**Credits: Audit**	**Contact Hours: 2**	
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**	
Teaching Hours: 25	**Examination Duration: -**		
Chapter 01:C language features Pointers revisited, Strings, Structures – Basics, Structures and functions, Arrays of structures, Pointers to structures, Self Referential Structures, Unions and bit fields, Files.			5 Hrs
Chapter 02:Stacks and Queues Definition, Representation and Applications of stack. Definitions, representation and applications of linear, circular, queues, multiple queues, priority queue. Recursion			5 Hrs

Chapter 03:Lists Linked lists, singly, doubly, circular lists, definitions, representations. Implementation of list operations, applications – polynomial addition, addition of long integers. Linked stacks, Linked Queues **Chapter 04:Trees** Binary trees – Definitions, traversals (recursive and iterative versions), Building and searching, Threaded Binary trees, Trees and their applications Exchange sorts, Selection and tree sorts, Merge and radix sorts	5 Hrs 5 Hrs 5 Hrs
Text Book 1. Aaron M. Tenenbaum, et al, Data Structures using C, II Edition, PHI, 2006 2. Horowitz, Sahani, Anderson-Feed, Fundamentals of Data Structures in C, II Edition, University, 2008 **References** 1. E Balaguruswamy, The ANSI C programming Language, II Edition, PHI, 2010 2. Yashavant Kanetkar, Data Structures through C, II Edition, BPB public, 2010 3. Richard F. Gilberg, Behrouz A. Forouzan , Data Structures: A Pseudocode Approach With C, II Edition, Course Tec, 2009	
Lab: **1.** Programs on Pointer concepts. **2.** Programs on string handling functions, structures union And bit-files. **3.** Programming on files **4.** Programming on stacks data structures **5.** Programs on implementation of different queue data structures. **6.** Programs on implementation of different types of Linked lists **7.** Programs on Implementation of trees **8.** Programs to implement different sorting techniques. **9.** Programming on graph **10.** Programming on hashing tables **11.** Design and implement stack queue data structures **12.** Design and implement linked list data structures **13.** project	

Program: Digital Electronics			
Course Title: Analog and Digital Circuits		**Course Code:** 17EDEC702	
L-T-P: 2-0-1	**Credits: 3**	**Contact Hours: 4**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 24	**Examination Duration: -**		
Applications of theorems. RLC Circuits Combinational circuits and Sequential circuits Case study Devices: Diodes, MOSFETs. Diode circuits: clipping, clamping, rectifier. Design of BJT and MOSFET single-and multi-stage amplifiers, Feedback amplifier, Oscillator, Op-amp linear & non linear applications. **Digital Circuits** Combinational Circuits: Adder, encoder & decoder, MUX& DEMUX, Comparator. Sequential Circuits: Latches, Flip Flops, Shift Registers, Design of Synchronous counters and Asynchronous counters. **Conventional control systems**: R-H Stability criterion, Root locus, Bode plots and Nyquist stability criterion. **Tools: Simulink, MATLAB, Proteus, Pspics, Cadence, LabView, Microcap, OrCAD**			8 Hrs 8 Hrs 8 Hrs

Reference Books:

1. A.S. Sedra & K.C. Smith, Microelectronic Circuits, 5th Edition, Oxford Univ. Press, 1999
2. Jacob Millman and Christos Halkias, Integrated Electronics, McGraw Hill,
3. John M Yarbrough, Digital Logic Applications and Design, Thomson Learning, 2001
4. David A. Bell, Electronic Devices and Circuits, 4th edition, PHI publication, 2007
5. Grey, Hurst, Lewis and Meyer, Analysis and design of analog integrated circuits, 4th edition.
6. Charles H Roth, Jr; Fundamentals of Logic Design, Thomson Learning, 2004.
7. Zvi Kohavi, Switching and Finite Automata Theory, 2ed, TMH
8. Ogata, Modern Control Theory, 4th ed, PHI.

Lab:

Analog Electronics Lab

1. Study & analyze Diode Clipping and Clamping (single/double ended) circuits.
2. Implement the RLC circuit to study the transient response.
3. Design an Amplifier using MOSFET and determine its gain, input & output impedance.
4. To implement an amplifier with negative feedback & show the effect of negative feedback on input impedance; output impedance & gain of the amplifier using MOSFET.
5. Study of transformer-less Class B push pull power amplifier and determination of its conversion efficiency
6. Design an amplifier for an unity gain and high input impedance using MOSFET. Suggest suitable techniques to increase the input impedance and verify the same.

Digital Circuits lab

1. Design and implement BCD adder and Subtractor using 4 bit parallel adder
2. Design and implement n bit magnitude comparator using 4- bit comparators
3. Design and implement Ring and Johnson counter using shift register.
4. Design and implement 8 bit ALU.

Tools: Simulink, Proteus, Pspics, Cadence, LabView, Microcap, OrCAD, MATLAB.

Program: I Semester Master of Technology (Digital Electronics)			**Teaching Hours**
Course Title: Principles of Embedded Systems		**Course Code: 17EDEC703**	
L-T-P: 0-0-2	**Credits: 2**	**Contact Hours: 4 Hrs/week**	
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**	
Teaching Hours: 42 Hrs	**Examination Duration:**		
1. Introduction to embedded system: Introduction, Classification of Embedded System, Major Application Areas, Purpose of Embedded System. Characteristics and quality attributes of Embedded Systems, Design Metric and Optimizing the metrics.			**06 Hrs**
2. Typical Embedded Systems: Core of Embedded System-processor fundamentals, up vs uc, risc vs cisc, vonneumann vs Harvard, 8051 controller architecture and programmer model, Memory, Sensor and Actuators, Communication Network, Embedded Firmware			**08 Hrs**
3. Low Level programming Concepts: Addressing Modes, Instruction Set and Assembly Language programming(ALP), Developing, Building, and Debugging ALP's			**08 Hrs**
4. Middle Level Programming Concepts: Cross Compiler, Embedded C language implementation, programming, & debugging, Differences from ANSI-C, Memory Models, Use of directives, Functions, Parameter passing and return types			**02 Hrs**
5. On-Chip Peripherals Study, Programming, and Application: Ports: Input/Output, Timers & Counters, UART, Interrupts			**08 Hrs**

6. External Interfaces Study, Programming and Applications : LEDS, Switches(Momentary type, Toggle type), Seven Segment Display: (Normal mode, BCD mode, Internal Multiplexing & External Multiplexing), LCD (8bit, 4bit, Busy flag, custom character generation), Keypad Matrix, Stepper Motor, DC Motor	**10 Hrs**

Text Books

1. Introduction to Embedded Systems 1E by Shibu K V.
2. Kenneth J. Ayala ; "The 8051 Microcontroller Architecture, Programming & Applications" 2e, Penram International, 1996 / Thomson Learning 2005
3. Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; "The 8051 Microcontroller and Embedded Systems – using assembly and C "- PHI, 2006 / Pearson, 2006

References

1. Embedded System Design: A Unified Hardware/Software Introduction – Frank Vahid, Tony Givargis, John Wiley & Sons, Inc.2002
2. Predko ; "Programming and Customizing the 8051 Microcontroller" –, TMH
3. Raj Kamal, "Microcontrollers: Architecture, Programming, Interfacing and System Design", Pearson Education, 2005

Program: Digital Electronics			**Teaching Hours**
Course Title: Fundamentals of signal processing		**Course Code: 17EDEC704**	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 5 Hrs/week**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 40 Hrs	**Examination Duration: 3 hrs**		
Chapter No. 1. Introduction Definition of a signals and systems, classification of signals, basic operation on signals, elementary signals, Systems viewed as Interconnection of operation, properties of systems.			**08 Hrs**
Chapter No. 2. Time-Domain representation for LTI systems Convolution, Impulse response representation, convolution sum and convolution integral. Properties of impulse response representation.			**08 Hrs**
Chapter No. 3. Discrete Fourier Transforms Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, its relationship with other transforms. use of DFT in linear filtering, overlap-save and overlap-add method. Fast-Fourier-Transform (FFT) need for efficient computation of the DFT (i.e. FFT algorithms). Radix-2 FFT algorithm for the computation of DFT and IDFT: decimation-in-time and decimation-in-frequency algorithms. Composite FFT.			**08 Hrs**
Chapter No. 4. Design of digital filters Design of digital filters: Considerations and Characteristics of practical digital filters. Design of digital filters: symmetric and anti symmetric FIR filters, design of linear phase FIR filters using windowing method- Rectangular, Hamming, Hanning, Bartlet and Kaiser windows. Design of linear phase FIR filters using frequency sampling technique.			**08Hrs**
Chapter No. 5. Design of IIR filters from analog filters Design of IIR filters from analog filters: Approximation of derivative, Impulse invariance method, bilinear transformation. Characteristics of commonly used Analog Filters: Butterworth and Chebyshev filters. Frequency transformation in the digital domain			**08Hrs**

Text Books

1. Simon Haykin and Barry Van Veen, Signals and Systems, second, John Wiley & Sons, 2002
2. Proakis & Monalakis, Digital signal processing Principles Algorithms & Applications, 4th Edition, PHI, New Delhi, 2007

References

1. Alan V. Oppenheim, Alan S Willsky and S. Hamid Nawab, Signals and Systems, second, Pearson Education Asia, 1997

Implementation Assignments:

1. Implementation assignments are designed using Python. Ex:
   - Generate different elementary signals and perform mathematical operations on them.
   - Calculate N point DFT and find the cost of computation, justify the use of FFT algorithms to calculate DFT.
   - Design Filters (FIR/IIR) for given specifications.
2. Explore the feature of SDR to build signal processing applications like,
   - Noise cancellation
   - Audio file editing

Program: I Semester Master of Technology (Digital Electronics)			**Teaching Hours**
Course Title: Machine learning		**Course Code: 17EDEC705**	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 5 Hrs/week**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 40 Hrs	**Examination Duration: 3 hrs**		
Chapter No. 1: Introduction Introduction What is Machine Learning? Applications of Machine Learning, Types of Machine Learning: Supervised, Unsupervised and Reinforcement learning, Dataset formats, Basic terminologies.			**05 Hrs**
Chapter No. 2: Supervised Learning Linear Regression, Logistic Regression Linear Regression: Single and Multiple variables, Sum of squares error function, The Gradient descent algorithm, Application, Logistic Regression, The cost function, Classification using logistic regression, one-vs-all classification using logistic regression, Regularization.			**10 Hrs**
Chapter No. 3: Supervised Learning: Neural Network Introduction to perception learning, Implementing simple gates XOR, AND, OR using neural network. Model representation, Gradient checking, Back propagation algorithm, Multi-class classification, Application- classifying digits, SVM.			**10 Hrs**
Chapter No. 4: Unsupervised Learning: Clustering Introduction, K means Clustering, Algorithm, Cost function, Application.			**05Hrs**
Chapter No. 5: Unsupervised Learning: Dimensionality reduction Dimensionality reduction, PCA- Principal Component Analysis. Applications, Clustering data and PCA.			**05Hrs**
Chapter No. 6: Machine Learning System Design Evaluating a hypothesis, Model selection, Bias and variance, error analysis, error metrics for skewed classes. Building a Model.			**05 Hrs**

Text Book (List of books as mentioned in the approved syllabus)

1. Tom Mitchell, Machine Learning, 1, McGraw-Hill. , 1997
2. Christopher Bishop, Pattern Recognition and Machine Learning, 1, Springer, 2007

References

1. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning : Data Mining, Inference and Prediction, 2, Springer, 2009

Implementation Assignments:

1. Assignments are designed to explore the concepts like
   - Supervise and unsupervised learning,
   - Clustering,
   - Regression and estimation
2. Motivate students to take up open challenges like Kaggle, walmart, ect

Program: I Semester Master of Technology (Digital Electronics)			**Teaching Hours**
Course Title: RISC Architectures		**Course Code: 17EDEC706**	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 3 Hrs/week**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 46 Hrs	**Examination Duration:**		
1. The 32 bit RISC Architecture: The Acorn RISC machine, Architectural inheritance, Architecture of ARM7TDMI, ARM programmers model, ARM development tools, 3 stage pipeline ARM organization, ARM instruction execution.			**06 Hrs**
2. 32 bit Instruction set: Data processing instruction, Branch instruction, Load store instruction, Software interrupt instruction, Program status register instruction, Conditional execution, Example programs, 16bit Instruction set- The Thumb programmer model, ARM-Thumb interworking, other branch instructions, Data processing instructions, Single/Multiple register load store instruction, Stack operation, Software interrupt instructions, example programs.			**06 Hrs**
3. Exception Handling: Introduction, Interrupts, error conditions, processor exception sequence, the vector table, Exception handlers, Exception priorities, Procedures for handling exceptions.			**04 Hrs**
4. Memory Hierarchy Design: Cache basics, Miss rate and penalty, Cache Hierarchy, Memory Organizations, Memory Hierarchy.			**06 Hrs**
5. Pipelining: Linear pipeline processor, Nonlinear pipeline processor, Instruction pipeline design, Branch handling techniques, Arithmetic pipeline design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipeline.			**08 Hrs**
6. Cortex M4 : Functional description, programmer's model, memory protection unit, nested vectored interrupt controller.			**06 Hrs**
7. Multi-Core Architectures : Introduction to Intel Architecture, How an Intel Architecture System works, Basic Components of the Intel Core 2 Duo Processor: The CPU, Memory Controller, I/O Controller.			**07 Hrs**
8. Current Trends in Intel Architectures and Applications :			**03 Hrs**

Seminar on current trends in Intel Architectures	

ext Books

1. "ARM System- on-Chip Architecture" by 'Steve Furber', LPE, Second Edition.
2. "ARM Assembly Language fundamentals and Techniques" by William Hohl, CRC press, 2009.
3. D. A. Patterson and J. L. Hennessey "Computer Organization and Design", Morgan , Kaufmann,2002
4. H. Jonathan Chao and Bin Liu, "High performance switches & routers", Wiley Interscience, 2007.
5. Kai Hwang, " Advanced Computer Architecture – TMH – 1993
6. Web resources for Example Architectures of INTEL and Texas Instruments: http:/ /download.intel.com/design/intarch/papers/321087.pdf

References

1. Kai Hwang, Faye A. Briggs, Computers Architecture and Parallel Processing – MGH – 1985
2. David E Culler, Jaswinder Pal Singh, Anoop Gupta "Parallel Computer Architecture", Harcourt Asia Pte Ltd 2000
3. Stalling W." Computer Organization and Architecture- Designing for performance" PHI,2005
4. D. Sima,T. Fountain, P.Kasuk," Advanced Computer Architecture-A Design Space Approach" Addisson Wesley,1997.
5. M. J. Flynn,"Computer Architecture, Pipelined And Parallel Processing", Narosa Publications, 1998.

List of Experiments:

1. Write an ALP to verify data transfer w.r.t memory to achieve following
   i. 8 bit data transfer
   ii. 16 bit data transfer
   iii. 32 bit data transfer
2. Write an ALP for Tables and lists to do following:
   i. Add an entry to a list
   ii. Remove an element from the queue
3. Write an ALP to pass parameters to a subroutine.
   i. Ascending order
   ii. Descending order
4. Write a 'C' program & demonstrate an interfacing of Alphanumeric LCD 2X16 panel to LPC2148Microcontroller
5. Write a 'C' program & demonstrate concept of Interrupts interface to LPC2148 Microcontroller.
6. Write a 'C' program & demonstrate an interfacing of DAC to LPC2148 Microcontroller.
7. Write a 'C' program & demonstrate an interfacing of UART to LPC2148 Microcontroller.
8. Write a 'C' program & demonstrate an interfacing of ADC to LPC2148 Microcontroller.
9. Write a 'C' program & demonstrate an interfacing of RTC to LPC2148 and read time, date and year.
10. Write a 'C' program & demonstrate interface I2C to LPC2148
11. Develop a code for college bell system. (Use the following interfaces LCD, RTC and Buzzer).

Reference Books

1. "ARM System- on-Chip Architecture" by 'Steve Furber", LPE, Second Edition.
2. "Embedded Systems- Architecture, Programming and Design" by Raj Kamal, TMH
3. Dr. K.V.K.K. Prasad, "Embedded/Real-time systems: concepts, Design & Programming", published by dreamtech press.

Manual

1. LPC2148 datasheet by NXP.
2. LPC2148 board manual by ALS, Bangalore.

Program: Digital Electronics		**Teaching Hours**
Course Title: Electronic System Design	**Course Code: 17EDEC707**	

L-T-P: 0-0-3	**Credits: 3**	**Contact Hours:6 Hrs/week**	
ISA Marks: 100	**ESA Marks:**	**Total Marks: 100**	
Teaching Hours: 25 Hrs	**Examination Duration: --**		
To level specifications, Block level specifications, Timing of micro architecture, Verification and test plan, Schematic capture			05 Hrs
Simulation, Advanced simulation, Signal Integrity			05 Hrs
PCB layout- Floor planning, component pre planning, PCB printing- 2 layer			05 Hrs
Functionality and performance check, Failure analysis, Validation and system integration			05 Hrs
System Analysis			05 Hrs

References

1. A. S Sedra and KC Smith, Microelectronic circuits, Oxford, 1998.
2. G.L. Ginsberg, Printed Circuit Design, McGraw Hill, 1991.

Program: Digital Electronics			
Course Title: Automotive Electronics		**Course Code:** 17EDEC708	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 5**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 40	**Examination Duration: 3 hrs**		
Chapter No. 1. Automotive Fundamentals Overview Introduction to Automotive Industry and Modern Automotive Systems Vehicle classifications and specifications need for electronics in automobiles, Application areas of electronics in the automobiles Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Spark pulse generation, Ignition Timing, Drive Train, Transmission, Brakes, Steering System.			8Hrs
Chapter No. 2. Sensors and Actuators Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor Strain gauge, Engine Coolant Temperature (ECT) Sensor, Knock Sensor, Throttle angle sensor, Fuel Injector Actuator, Ignition Actuator			7Hrs
Chapter No. 3. Electronic Engine Control Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle sped control, EGR Control			5Hrs
Chapter No. 4. Vehicle Motion Control and Safety Systems Cruise Control, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronic Stability Program.			6Hrs
Chapter No:5. Automotive communication protocols Overview of Automotive communication protocols : CAN, LIN .			3Hrs
Chapter No. 6. Advanced Driver Assistance Systems (ADAS) Lane Departure Warning, Collision Warning, Automatic Cruise Control, Pedestrian Protection, Headlights Control, Connected Cars technology and trends towards Autonomous vehicles.			5Hrs

Chapter No. 7. Automotive safety standards ISO26262 and Diagnostics Functional Safety: Need for safety standard-ISO 26262, safety concept, safety process for product life cycle, safety by design, validation. Fundamentals of Diagnostics: Basic wiring system and Multiplex wiring system, Preliminary checks and adjustments, Self-diagnostic system. Fault finding and corrective measures, OBD & off board diagnostic.	6Hrs

Text books:

1. Denton.T – Automobile Electrical and Electronic Systems, Edward Arnold publication, 1995.

References:

1. William T.M – Automotive Electronic Systems, Heiemann Ltd., London ,1978.
2. Nicholas Navet – Automotive Embedded System Handbook, CRC Press, 2009.
3. BOSCH Automotive Handbook, Wiley Publications, 8th Edition, 2011.
4. Co-Verification of hardware & software for ARM SoC Design – Jason.R.Andrews, Newnes Publications, 2004.
5. Hardware Software co-design of embedded systems, F.Balarin, Kluwer Academic Oublishers, 1987.

Lab:

1. Demonstration of cut section modules: Engine, Transmission , Steering, Braking, Suspension - Automobile dept.
2. Electronic engine control system: Injection and Ignition control system Transmission trainer modules
3. Modeling an engine Vehicle model simulation with Simulink using PI CONTROLLER
4. Basic gate logic simulation and modeling using Simulink and realization on the hardware platform.
5. Seat belt warning system simulation and modeling using Simulink and realization on the hardware platform. Vehicle speed control based on the gear input simulation and modeling using Simulink and realization on the hardware platform.
6. Throttle control modeling and simulation using Simulink and realization on the hardware platform.
7. Accelerator pedal interfacing software modeling and simulation using Simulink and realization on the hardware platform.
8. Develop matlab code for stepper motor control and convert it to Simulink model and port it to embedded hardware

KLE Technological University Creating Value Leveraging Knowledge	School of Electronics & Communication Engineering **PG – Digital Electronics**

Course Code: **17EDEC710**	Course Title: **Multimedia and Signal Processing**		Teaching Hrs: **40 Hrs**
L-T-P: **3-0-1**	Credits: **4**		Contact Hrs: **5 Hrs/week**
ISA Marks: **50+100**	Exam Duration: **3Hrs**	ESA Marks: **50**	Total Marks: 2**00**

1	**Introduction to Multimedia:** Multimedia and Hyper media, WWW, overview of multimedia software tools.	**02Hrs**
2	**Graphics and Image representation:** Graphics / Image data types, Popular file formats.	**02Hrs**
3	**Fundamental concepts in video:** Types of video signals, analog video, digital video.	**06Hrs**
4	**Basics of digital audio:** Digitization of sound, MIDI, Quantization and transmission of audio.	**05Hrs**
5	**Lossless compression algorithms:** Introduction, run-length coding, variable length coding, dictionary based coding, arithmetic coding, lossless image compression.	**05Hrs**
6	**Lossy compression algorithms:** Introduction, distortion measures, quantization, transform coding, wavelet based coding, wavelet packets, embedded zero tree of wavelet coefficients.	**06Hrs**
7	**Image compression standards:** The JPEG standard, The JPEG2000 standard, The JPEG-LS standard, Bi level image compression standard.	**06Hrs**
8	**Basics video compression techniques:** Overview, video compression based on motion compensation, H.261 .	**08Hrs**

Text books

1. Ze-Nian Li & Mark S Drew**, "**Fundamentals of multimedia**"**, Pearson Education, 2004.

References books

1. Ralf Steinmetz & Kalra Nahrstedt , "Multimedia: Computing, Communication & Applications", Pearson Education, 2004

2. K R Rao, Zoran S Bojkovic, Dragord A Milovanvic, Pearson education, "Multimedia communication systems: Techniques, Standards, & Networks",. Second Indian reprint, 2004.

Course Code: 17EDEC711	**Course Title: Data Communication**	
L-T-P: 3-0-1	**Credits: 4**	**Contact Hrs: 5 hrs/week**
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**
Teaching Hrs: 40		**Exam Duration: 03 hrs**

Content	**Hrs**
Chapter No. 1. Computer Networks and the Internet What is Internet? The Network Edge, the network Core,delay -loss—throughput in packet switched	06hrs

networks. Protocol layers (OSI layers) and their service models.	
Chapter No. 2. Application Layer Principles of network applications,the web and HTTP,DHCP, file transfer-FTP,electronic mail in the internet,DNS,peer-to-peer applications.	10hrs
Chapter No. 3. Transport Layer Introduction and transport-layer services-relationship between transport and network layers - overview of the transport layer in the internet, multiplexing and de multiplexing, connectionless transport: UDP, principles of reliable data transfer, connection oriented transport TCP, TCP congestion control.	08hrs
Chapter No. 4. Network layer Introduction, virtual circuit and datagram networks, what's inside router? The Internet protocol (IP): forwarding and addressing in the internet, routing algorithms, routing in the internet, broadcast and multi cast routing.	08hrs
Chapter No. 5. The link layer: Links, Access networks, and LANs Introduction to the link layer, error-detection and correction techniques, multiple access links and protocols, switched local area networks, link virtualization: A network as a link layer, data center networking.	08hrs

Text Book (List of books as mentioned in the approved syllabus)

1. Kurose & Ross, Computer Networking A Top-Down Approach, 6th editionPEARSON, 2013.

References

1. Larry L. Peterson & Bruce S. Davie, Computer Networks: A Systems Approach, 4th edition, Elsevier, 2004
2. Behrouz A. Forouzan, Data Communication and Networking, 4th edition, TMG, 2002

Lab:

1. Introduction to Hardware components and Ethernet LAN set up.
2. Introduction to socket programming
3. Implementation of FTP
4. Implementation of error control techniques.
5. Implementation of flow control ARQs
6. Introduction to Network operating system.
7. Subnet design
8. VLAN setup
9. OSPF and RIP configuration and performance analysis
10. eBGP and iBGP configuration and performance analysis

Text Book

1. Kurose & Ross, Computer Networking A Top-Down Approach, 6th editionPEARSON, 2013.

References

1. Cisco networking academy, https://www.netacad.com/
2. Juniper networking academy, https://learningportal.juniper.net/

KLE Technological University — Creating Value, Leveraging Knowledge	School of Electronics & Communication Engineering **PG – Digital Electronics**

Course Code: **17EDEE701**	Course Title: **Image and Video Processing**		Teaching Hrs: **40 Hrs**
L-T-P: **2-0-1**	Credits: **3**		Contact Hrs: **4 Hrs/week**
ISA Marks: **50+100**	Exam Duration: **3Hrs**	ESA Marks: **50**	Total Marks: **100**

1	**Introduction**: 2D systems, Mathematical Preliminaries- FT, Z-transform, Optical and Modulation Transfer Functions (OTF and MTF). Matrix theory, Image perception: Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome Vision Models, Fidelity criteria, Color Representation, Color Vision Models, Temporal Properties of Vision.	2 hrs
2	**Image sampling and Quantization:** 2D Sampling theory, Quantization, Optimal Quantizer, Compander and Visual Quantization.	2 hrs
3	**Image Transforms:** 2D orthogonal and unitary transforms, DFT, DCT, Harr, KLT	4hrs
4	**Image Enhancement**: Histograms Modeling, Spatial operations, Transform operations, Multispectral Image Enhancement,	4hrs
5	**Image Filtering and Restoration:** Image Observation Models, Inverse and Weiner filtering , Frequency Domain Filters. Smoothing Splines and Interpolation.	4hrs
6	**Basics of Video:** Analog Video, Digital Video	2 hrs
7	**Two dimensional motion estimation:** Optical flow methods**,** Block based methods, Bayesian methods**.**	7 hrs

Text books

1. Jain, A.K., Fundamentals of Digital Image Processing, 3rd Edision, Pearson Education (Asia) 2013
2. A. Murat Tekalp, Digital Video processing Pearson Education (Asia) Pte. Ltd.
3. Li and, Z. Drew, M.S. Fundamentals of Multimedia, Pearson Education (Asia) Pte. Ltd,. 2010.

References books

1. Gonzalez, Rafael C., Woods, Richard E. and Eddins Steven L., Digital Image Processing Using Matlab, Pearson Education (Asia) Pvt. Ltd.,
2. Al. Bovik, Essential guide to Video Processing, Academic Press

Program: Digital Electronics		
Course Title: Digital Control Systems		**Course Code:** 17EDEE702
L-T-P: 2-0-1	**Credits: 4**	**Contact Hours: 5**
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40	**Examination Duration: 3 hours**	

1. Introduction to digital control: Introduction, Discrete time system representation, Mathematical modeling of sampling process, Data reconstruction.	4hrs
2. Modeling discrete-time systems by pulse transfer function: Z-transform, Mapping of Z-plane to z-plane, Pulse transfer function , Pulse transfer function of closed loop system, Sampled signal flow graph.	3hrs
3. Time response of discrete systems: Transient and steady state responses, Time response parameters of a prototype second order system.	5hrs
4. Stability analysis of discrete time systems: Jury stability test, Stability analysis using bi-linear transformation.	
5. Design of sampled data control systems: Root locus method, Controller design using root locus, Root locus based controller ,design using MATLAB, Nyquist stability criteria, Bode plot.	5hrs
6. Deadbeat response design :Design of digital control systems with deadbeat response, Practical issues with deadbeat response design, Sampled data control systems with deadbeat response.	5hrs
7. Discrete state space model: Introduction to state variable model, Various canonical forms, Characteristic equation, state transition matrix, solution to discrete state equation.	6hrs
8. Controllability, observability and stability of discrete state space models: Controllability and observability, Lyapunov stability theorem.	2hrs
9. State feedback design: Pole placement by state feedback, Set point tracking controller, Full order observer, Reduced order observer.	5hrs
	5hrs

References:

1. B. C. Kuo,Digital Control Systems, Oxford University Press, 2/e, Indian Edition, 2007.
2. K. Ogata, Discrete Time Control Systems, Prentice Hall, 2/e, 1995.
3. M. Gopal,Digital Control and State Variable Methods, Tata Mcgraw Hill, 2/e, 2003.
4. G. F. Franklin, J. D. Powell and M. L. Workman, Digital Control of Dynamic Systems,

Program: Digital Electronics		
Course Title: Multi Sensor Data Fusion		**Course Code:** 17EDEE703
L-T-P: 2-0-1	**Credits: 4**	**Contact Hours: 5**
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40	**Examination Duration: 3 hours**	

Chapter 1: **Fundamentals of Multi-sensor data Fusion system** Multi sensor data fusion strategies, formal framework, catastrophic fusion, Smart sensor, logical sensor, interface file system, sensor observation, sensor characteristics, sensor-sensor properties, Fusion node, simple fusion network, network topology.	**08 hours**
Chapter 2: Sensor modeling Mathematical modeling, Baye's Theorem, sensor modeling, sensor data normalization, Neural network approach.	**06 hours**
Chapter 3: State –Estimation techniques State-space approach: State-space representation, Time response of homogeneous systems: Kalman filtering: practical aspects of Kalman filtering, Applications	**06 hours**
Chapter 4: Representation Spatial-temporal transformation, geographical information system, common representation format, subspace methods, multiple training sets.	**06 hours**
Chapter 5: Spatial alignment Image registration, resample/interpolation, pair wise transformation, image fusion, mosaic image. .	**06 hours**
Chapter 6: Temporal alignment & Semantic alignment Dynamic time warping, dynamic programming, video compression, assignment matrix for semantic alignment, clustering algorithms	**06 hours**
Chapter 7: Data fusion: Bayesian Interface, Bayesian analysis, probability model, Posteriori distribution, Model selection, computation.	**06 hours**
Chapter 8: **Sensor management:** Hierarchical classification, sensor management techniques.	**06 hours**
Text Books: 1. H.B.Mitchell, "Multi Sensor Data Fusion, An Introduction" Springer,2007. 2. David L. Hall, Mathematical techniques in Multisensor data fusion, Artech House,Boston. 3. Madan Gopal, Digital control and state variables methods 2nd edition, PHI 4. Pattern Recognition and Machine Learning" by Christopher M. Bishop	

Program: III Semester Master of Technology (Digital Electronics)			**Teaching Hours**
Course Title: Embedded Software Design		**Course Code: 17EDEC801**	
L-T-P: 0-0-3	**Credits: 3**	**Contact Hours: 6 Hrs/week**	
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**	
Teaching Hours: 40 Hrs	**Examination Duration:**		

1. Introduction To Real-Time Operating Systems: Introduction to OS, Introduction to real time embedded system- real time systems, characteristics of real time systems, and the future of embedded systems. Introduction to RTOS, key characteristics of RTOS, its kernel, components in RTOS kernel, objects, scheduler, services, context switch, Scheduling types: Preemptive priority-based scheduling, Round-robin and preemptive scheduling.	**08 Hrs**
2. Tasks, Semaphores and Message Queues:: A task, its structure, A typical finite state machine, Steps showing the how FSM works. A semaphore, its structure, binary semaphore, mutual exclusion (mutex) semaphore, Synchronization between two tasks and multiple tasks, Single shared-resource-access synchronization, Recursive shared-resource-access synchronization. A message queue, its structure, Message copying and memory use for sending and receiving messages, Sending messages in FIFO or LIFO order, broadcasting messages.	**08 Hrs**
3. Typical RTOSs: Study of VX works, RT Linux and Android OS and comparisons. Real time programming using RTX/free RTOS. Applications and Common Design Problems: Embedded RTOS for Image Processing & Control Systems, and common problems encountered in these applications.	**04 Hrs**
4. Introduction to embedded linux: Embedded Linux overview: Development-Kernel architectures and device driver model-Embedded development issues-Tool chains in Embedded Linux-GNU Tool Chain (GCC,GDB, MAKE, GPROF & GCONV)- Linux Boot process	**02 Hrs**
5. Boot sequence-System loading, sys linux, Lilo, grub-Root file system-Binaries required for system operation-Shared and static Libraries overview-Writing applications in user space-GUI environments for embedded Linux system	**02 Hrs**
6. File system in Linux: File system Hierarchy-File system Navigation -Managing the File system –Extended file systems-INODE-Group Descriptor-Directories-Virtual File systems-Performing File system Maintenance - Locating Files –Registering the File systems-Mounting and Un-mounting –Buffer cache-/proc file systems-Device special files	**08 Hrs**
7. Program design and Analysis : Components of Embedded system: State machines; stream oriented programming and circular buffers, queues. Models of programs: data flow graph and control flow graphs, Assembly, linking and loading. Basic compilation techniques: Statement translation, procedures, data structures. Program optimization: Expression simplification, dead code elimination, procedure inlining, loop transformations, register allocation, scheduling, instruction selection, interpreters and JIT compilers. Program level performance analysis, software performance optimization, program level energy and power analysis, analysis and optimization of program size. Program validation and testing: Clear box testing, black box testing, evaluating function tests.	**08 Hrs**

Text Books

1. Qing Li with Caroline Yao, “Real-Time Concepts for Embedded Systems”, Published by CMP Books,2011
2. Dr. K.V.K.K. Prasad, “Embedded/Real-time systems: concepts, Design & Programming”, published by dreamtech press .
3. “Embedded Systems- Architecture, Programming and Design” by Raj Kamal, TMH

References

1. Philip.A.Laplante, “Real Time System Design and Analysis”, Prentice Hall of India, 3rd Edition, April 2004.
2. “Programming embedded systems” in C and C++ Micheal Barr orielly

List of Experiments:

1. Write a ‘C’ program & demonstrate concept of Task Scheduling.
2. Write a ‘C’ program & demonstrate concept of Semaphore.
3. Write a ‘C’ program & demonstrate concept of Mailbox.
4. Write a ‘C’ program & demonstrate concept of S/W Interrupts.
5. Write a ‘C’ program & demonstrate concept of interrupts.
6. Write a ‘C’ program & demonstrate concept of Inter Task Communication.

Reference Books

1. Dr. K.V.K.K. Prasad, “Embedded/Real-time systems: concepts, Design & Programming”, published by dreamtech press.

Manual

1. LPC2148 datasheet by NXP.

LPC2148 board manual by ALS, Bangalore.

Program: Digital Electronics		
Course Title: Automotive Communication		Course Code: 17EDEC802
L-T-P: 3-0-0	Credits: 3	Contact Hrs: 3
CIA Marks: 50	SEE Marks: 50	Total Marks: 100
Teaching Hrs: 40	Exam Duration: 3 hrs	

Content	**Hrs**
Chapter No. 1: Controller Area Network Introduction to CAN, Basic Concepts, Message Transfer, Frame Types, Message Validation, Error Handling, Fault Confinement, Bit Timing Requirements, Increasing Can Oscillator Tolerance, Protocol Modifications.	15 hrs
Chapter No. 2: Local Interconnect Network Overview of LIN protocol, LIN Workflow ,LIN Physical Layer ,LIN Communication, Synchronization of the LIN nodes, LIN Message & Scheduling, Message Types, Status & Network Management, Introduction to LIN slave diagnostics , Introduction to LIN slave configuration.	5 hrs
Chapter No. 3: Flexray Communication protocol Introduction to Fleray, Basic Concepts, Message Transfer, Static and dynamic data transmission, Flexray BUS, FlexRay controller states, Frame Types, Message Validation, Error Handling, Fault Confinement, Bit Timing Requirements, Fault tolerant and time triggered services implemented in hardware.	5 hrs
Chapter No. 4: Media oriented system transport protocol Technology background, MOST25, MOST50, MOST150, MOST topology, different masters in MOST	5 hrs

network, control channel, synchronous channel, asynchronous channel, MOST application frame work, addressing scheme, frame formats,	
Chapter No. Chapter 5: Keyword 2000 protocol Overview of KWP protocol, KWP Workflow , Physical topology ,message structure, frame format,	5 hrs
Chapter No. Chapter 6: SENT, I2C, SPI and UART Overview about SENT , I2C, SPI and UART, frame formats, application of I2C, SPI, SENT and UART in automotive.	5 hrs
Text Books (List of books as mentioned in the approved syllabus) Ronald K. Jurgen, Infotainment systems, 2007, SAE International, 2007	

Program: III Semester Master of Technology (Digital Electronics)			**Teaching Hours**
Course Title: Internet of Things		**Course Code: 17EDEE801**	
L-T-P: 2-0-1	**Credits: 3**	**Contact Hours: 5 Hrs/week**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 200**	
Teaching Hours: 25 Hrs	**Examination Duration:**		

1	**Introduction to Internet of Things (IoT)** Definition & Characteristics of IoT, Things in IoT, IoT protocols, IoT functional blocks, communication models and APIs.	**04 hrs**
2	**IoT Architecture** Enabling technologies: Sensors, Zigbee, Bluetooth, IoT ecosystem, Data Link protocols: IEEE 802.15.4e, IEEE 802.11.ah, DASH7, Low Power Wide Area Network (LoRaWAN).	**04 hrs**
3	**Network protocols** Routing Protocol for Low-Power and Lossy Networks (RPL), cognitive RPL (CORPL), Channel-Aware Routing Protocol (CARP), Low power Wireless Personal Area Networks (LoWPAN).	**04 hrs**
4	**Application and Security protocols** Message Queue Telemetry Transport (MQTT), MQTT for Sensor Networks, Secure MQTT, Advanced Message Queuing Protocol (AMQP), Constrained Application Protocol (CoAP), OPC UA, 6LoWPAN), Routing Protocol for Low-Power and Lossy Networks (RPL).	**04 hrs**
5	**IoT Platforms Design Methodology** IoT Design Methodology, Case Study on IoT System for Weather Monitoring etc., Basic building blocks of an IoT device, Raspberry Pi, interface (serial, SPI, I2C), IoT Operating Systems: Contiki, RIOT.	**04 hrs**
6	**Programming with Raspberry Pi** XML, JSON, SOAP and REST-based approach, WebSocket protocol.	**04 hrs**
7	**IoT prototyping** Business models, example applications: Case studies on Home automation, Cities, Environment, Energy, Agriculture, Health with emphasis on data analytics and security.	**06 hrs**

Text Books:

1. Arshdeep Bahga, Vijay Madisetti “Internet of Things (A Hands-on-Approach)” Universities Press- 2014.
2. Olivier Hersent, David Boswarthick, Omar Elloumi, “The Internet of Things: Key Applications and Protocols”

John Wiley & Sons – 2012.

Reference Books:

1. Subhas Chandra Mukhopadhyay “Internet of Things Challenges and Opportunities” Springer- 2014.

Lab:

1. Programming with Raspberry Pi
2. Cloud service interface for data storage and retrieval
3. Performance analysis of Data link protocols, routing and application protocols
4. Open Ended Experiment with focus on data analytics and security

Course Code: 17EDEE802	Course Title: AUTOSAR	
L-T-P : 2-0-1	Credits: 3	Contact Hrs: 3 Hours
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3

Content	Hrs
Unit - 1	
Chapter No. 1: AUTOSAR Fundamentals Evolution of AUTOSAR – Motivations and Objectives AUTOSAR consortium – Stake holders – work Packages, AUTOSAR Partnership, Goals of the partnership, Organization of the partnership, AUTOSAR specification, AUTOSAR Current development status, BSW Conformance classes: ICC1, ICC2, ICC3, and Drawbacks of AUTOSAR.	8 hrs
Chapter No. 2: AUTOSAR layered Architecture AUTOSAR Basic software, Details on the various layers , Details on the stacks Virtual Function Bus (VFB) Concept Overview of AUTOSAR Methodology , Tools and Technologies for AUTOSAR AUTOSAR Application Software Component (SW-C) ,Types of SW-components AUTOSAR Run Time Environment (RTE): RTE Generation Process: Contract Phase, Generation Phase, MCAL, IO HW Abstraction Layer, Partial Networking, Multicore, J1939 Overview, AUTOSAR Ethernet, AUTOSAR E2E Overview , AUTOSAR XCP, Metamodel , From the model to the process , Software development process.	7 hrs
Unit - 2	
Chapter No. 3: Methodology of AUTOSAR and Communication in AUTOSAR CAN Communication, CAN FD, CAN in Automation, CANape, Application Layer and RTE, intra and inter ECU communication, Client-Server Communication, Sender-Receiver, Communication, CAN Driver, Communication Manager (ComM), Overview of Diagnostics Event and Communication Manager	10 hrs
Chapter No. 4: BSW Development and Integration BSW Constituents: Memory layer, COM and Services layer, ECU abstraction, AUTOSAR, Operating system, Interfaces: Standard interface, AUTOSAR standardized interface, BSW-RTE interface,(AUTOSAR interface), BSW-ECU hardware interface, Complex device drivers and BSW module configuration, AUTOSAR Integration.	5 hrs
Unit - 3	
Chapter No. Chapter 5: Infotainment Systems in Automobiles Infotainment Systems Fundamentals: Radio, Multimedia, and Navigation: Introduction to In Vehicle	5 hrs

Infotainment (IVI) systems, Use of operating systems in IVI , GENIVI Alliance, Tuner: AM/FM, XM/Sirrus, DAB/DMB, Software Defined Radio; Concepts of HD, radio, Ensemble, Traffic Announcements, Spread Spectrum, d. Multimedia: Types of Media; Music, Video, Podcasts, etc. Media management; Playback, Track Control, Metadata, Playlists, Categories, Trick play, Audio/Video Source Management, Navigation: Points of Interests, Routes, Waypoints, Dead Reckoning position, Traffic Info, GLONASS, GNSS, RTK, GPS, and SBAS/GBAS,INS f. Media types: CD, DVD, CDDA, USB, SDCARD, Media Formats:MP3, WMV, RealAudio/Video, QTP, Architecture – Design Patterns - Proxies, Adaptors, Interfaces, Singleton, Factory method	
Chapter No. Chapter 6: Communication Systems in Automobiles Automotive & Consumer Electronic Communication Systems: Introduction to Bluetooth – Pairing, HFP, A2DP, PAN, PBAP, DUN, Concepts of MOST network, DLNA, AVB, Concepts of TCP/IP, Ethernet, WiFi, WiFi Direct, MyWiFi and CAN, Mirror link, Tethering	5 hrs
Text Book (List of books as mentioned in the approved syllabus) 1. Ribbens, Understanding of Automotive electronics, 6th Edition, Elsevier, 2003 2. Denton.T, Automobile Electrical and Electronic Systems, Elsevier, 3rd Edition, 2004 3. Denton.T, Advanced automotive fault diagnosis, 2000 **References** 1. Ronald K Jurgen, Automotive Electronics Handbook, 2nd Edition, McGraw-Hill, 1999 2. James D Halderman, Automotive electricity and Electronics, PHI Publication, 2000 3. Allan Bonnick, Automotive Computer Controlled Systems Diagnostic Tools and Techniques, Elsevier Science, 2001 4. Nicholas Navet , Automotive Embedded System Handbook , 2009	

Program: III Semester Master of Technology (Digital Electronics)			**Teaching Hours 04 hrs**
Course Title: Multirate Signal Processing		**Course Code: 17EDEE803**	
L-T-P: 2-0-1	**Credits: 3**	**Contact Hours: 5 Hrs/week**	
ISA Marks: 50+100	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 25 Hrs	**Examination Duration: 3 hrs**		

Chapter No. 1. Introduction Definition of a signals and systems, classification of signals, basic operation on signals, elementary signals, Systems viewed as Interconnection of operation, properties of systems.	**08 Hrs**
Chapter No. 2. Time-Domain representation for LTI systems Convolution, Impulse response representation, convolution sum and convolution integral. Properties of impulse response representation.	**08Hrs**
Chapter No. 3. Discrete Fourier Transforms Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, its relationship with other transforms. use of DFT in linear filtering, overlap-save and overlap-add method. Fast-Fourier-Transform (FFT) need for efficient computation of the DFT (i.e. FFT algorithms). Radix-2 FFT algorithm for the computation of DFT and IDFT: decimation-in-time and decimation-in-frequency algorithms. Composite FFT.	**08 Hrs**
Chapter No. 4. Design of digital filters Design of digital filters: Considerations and Characteristics of practical digital filters. Design of digital filters: symmetric and anti symmetric FIR filters, design of linear phase FIR filters using windowing method- Rectangular, Hamming, Hanning, Bartlet and Kaiser windows. Design of linear phase FIR filters using frequency sampling technique.	**08Hrs**

Chapter No. 5. Design of IIR filters from analog filters Design of IIR filters from analog filters: Approximation of derivative, Impulse invariance method, bilinear transformation. Characteristics of commonly used Analog Filters: Butterworth and Chebyshev filters. Frequency transformation in the digital domain	**08Hrs**

Text Books

3. Simon Haykin and Barry Van Veen, Signals and Systems, second, John Wiley & Sons, 2002
4. Proakis & Monalakis, Digital signal processing Principles Algorithms & Applications, 4th Edition, PHI, New Delhi, 2007

References

2. Alan V. Oppenheim, Alan S Willsky and S. Hamid Nawab, Signals and Systems, second, Pearson Education Asia, 1997

Implementation Assignments:

3. Implementation assignments are designed using Python. Ex:
   - Generate different elementary signals and perform mathematical operations on them.
   - Calculate N point DFT and find the cost of computation, justify the use of FFT algorithms to calculate DFT.
   - Design Filters (FIR/IIR) for given specifications.
4. Explore the feature of SDR to build signal processing applications like,
   - Noise cancellation
   - Audio file editing

Program: Digital Electronics			**Teaching Hours**
Course Title: Advanced Computer Architecture & Programming		**Course Code: 17EDEC801**	
L-T-P: 2-0-1	**Credits: 3**	**Contact Hours: 4 Hrs/week**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 40 Hrs	**Examination Duration: 3 hrs**		
Chapter 1: Instructions: Representing Instructions in the Computer, ARM Addressing for 32-Bit Immediates and more complex addressing modes, Parallelism and Instructions: Synchronization, Translating and Starting a Program.			**05**

Chapter 2: Arithmetic for Computers Addition and Subtraction, Multiplication, Division, Floating Point, Parallelism and Computer Architecture: Associativity.	**05**
Chapter 3: The Processor: Introduction, Logic Design Conventions, Building a Datapath , A Simple Implementation Scheme, An overview of pipelining, Pipelined datapath and control, Data Hazards: Forwarding versus Stalling, Control hazards, Exceptions , Parallelism and advanced instruction level parallelism, Real Stuff: AMD opteron pipeline, Advance Topic: an introduction to describe and model a pipeline and more pipelining illustrations.	**10**
Chapter 4: Large and Fast: Exploiting Memory Hierarchy Introduction, The Basics of Caches , Measuring and Improving Cache Performance, Virtual Memory A Common Framework for Memory Hierarchies, Virtual machines, using a finite state machine to control a simple cache, Parallelism and memory hierarchy: cache coherence ,Advanced material: Implementing cache controllers, Real Stuff: AMD Opteron & Intel Nehalem Memory hierarchies	**10**
Chapter 5: Storage, Networks, and Other Peripherals Introduction , Dependability, Reliability and Availability, Disk Storage, Flash storage, Connecting Processors, Memory, and I/O Devices, Interfacing I/O Devices to the Processor, Memory and Operating System, I/O Performance Measures: Examples from Disk and File Systems, Designing an I/O System, Parallelism and I/O: Redundant arrays of inexpensive disks, Real Stuff: Sun firwe x4150 server, Advanced topics: Networks	**10**
Chapter 6: Multicores, Multiprocessors and Clusters Introduction, Difficulty of creating parallel processing programs, Shared memory multiprocessors Clusters and other message passing multiprocessors,Hardware multithreading,SISD, MIMD, SIMD, SPMD, and vector,Introduction to graphics processing units,Introduction to multiprocessor network topologies, Multiprocessor benchmarks, Roofline : A simple performance model, Real Stuff: Benchmarking four multicores using the roofline model.	**10**

Text Books:

1. Computer Organization and Design, The hardware/Software interface, ARM edition– David A. Patterson, John L.Hennessy. 4th edition,MK publishers,2009

Reference Books:

1. Computer Architecture and Organization- John P. Hayes, 3rd edition, McGraw-Hill, 1998

Program: Digital Electronics			
Course Title: AUTOSAR and Infotainment Systems		Course Code: **17EDEE801**	
L-T-P : 2-0-1	Credits: 3	Contact Hrs: 4	
CIA Marks: 50	SEE Marks: 50	Total Marks: 100	
Teaching Hrs: 24	Exam Duration: 3 hrs		
Chapter No. 1: AUTOSAR Fundamentals Evolution of AUTOSAR – Motivations and Objectives AUTOSAR consortium – Stake holders – work Packages, AUTOSAR Partnership, Goals of the partnership, Organization of the partnership, AUTOSAR specification, AUTOSAR Current development status, BSW Conformance classes: ICC1, ICC2, ICC3, and Drawbacks of AUTOSAR.			4 hrs

Chapter No. 2: AUTOSAR layered Architecture AUTOSAR Basic software, Details on the various layers , Details on the stacks Virtual Function Bus (VFB) Concept Overview of AUTOSAR Methodology , Tools and Technologies for AUTOSAR AUTOSAR Application Software Component (SW-C) ,Types of SW-components AUTOSAR Run Time Environment (RTE): RTE Generation Process: Contract Phase, Generation Phase, MCAL, IO HW Abstraction Layer, Partial Networking, Multicore, J1939 Overview, AUTOSAR Ethernet, AUTOSAR E2E Overview , AUTOSAR XCP, Metamodel , From the model to the process , Software development process.	4 hrs
Unit - 2	
Chapter No. 3: Methodology of AUTOSAR and Communication in AUTOSAR CAN Communication, Application Layer and RTE, intra and inter ECU communication, Client-Server Communication, Sender-Receiver, Communication, CAN Driver, Communication Manager (ComM), Overview of Diagnostics Event and Communication Manager	4 hrs
Chapter No. 4: BSW Development and Integration BSW Constituents: Memory layer, COM and Services layer, ECU abstraction, AUTOSAR, Operating system, Interfaces: Standard interface, AUTOSAR standardized interface, BSW-RTE interface,(AUTOSAR interface), BSW-ECU hardware interface, Complex device drivers and BSW module configuration, AUTOSAR Integration.	4 hrs
Chapter No. Chapter 5: Infotainment Systems in Automobiles Infotainment Systems Fundamentals: Radio, Multimedia, and Navigation: Introduction to In Vehicle Infotainment (IVI) systems, Use of operating systems in IVI , GENIVI Alliance, Tuner: AM/FM, XM/Sirrus, DAB/DMB, Software Defined Radio; Concepts of HD, radio, Ensemble, Traffic Announcements, Spread Spectrum, d. Multimedia: Types of Media; Music, Video, Podcasts, etc. Media management; Playback, Track Control, Metadata, Playlists, Categories, Trick play, Audio/Video Source Management, Navigation: Points of Interests, Routes, Waypoints, Dead Reckoning position, Traffic Info, GLONASS, GNSS, RTK, GPS, and SBAS/GBAS,INS f. Media types: CD, DVD, CDDA, USB, SDCARD, Media Formats:MP3, WMV, RealAudio/Video, QTP, Architecture – Design Patterns - Proxies, Adaptors, Interfaces, Singleton, Factory method	4 hrs
Chapter No. Chapter 6: Communication Systems in Automobiles Automotive & Consumer Electronic Communication Systems: Introduction to Bluetooth – Pairing, HFP, A2DP, PAN, PBAP, DUN, Concepts of MOST network, DLNA, AVB, Concepts of TCP/IP, Ethernet, WiFi, WiFi Direct, MyWiFi and CAN, Mirror link, Tethering	4 hrs
Text Books 1. Ronald K. Jurgen, Infotainment systems, 2007, SAE International, 2007	