Program: III Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Engineering Design		**Course Code: 17EECF201**	
L-T-P: 0-0-3	**Credits: 3**	**Contact Hours: 03 Hrs/week**	
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**	
Teaching Hours:	**Examination Duration: 2 Hrs**		
PART A			
Planning Introduction to Engineering Design, Problem Definition, Design attributes Gantt Chart, Design Objectives, Design Specifications			**02**
Conceptual Design Functional Analysis, Concept generation, Concept Evaluation			**03**
System Level Design Product Architecture, Configuration Design, Parametric Design			**03**
Detail Design Sub-system Design, Design Verification			**03**
PART B			
OrCAD Functional simulation of basic Analog and Digital application circuits using OrCAD eCAD tool			**01**
Schematic Capture of the reference design using using OrCAD eCAD tool.			**01**
Layout Design of the reference design using using OrCAD eCAD tool.			**01**
Creation of Symbols/Cell/Part			**01**
LabVIEW Introduction to LabVIEW and functional simulation of basic Analog and Digital application circuits in LabVIEW			**01**
Functional Simulation of the circuit for selected problem statement			**01**
Co-simulation of the circuit for selected problem statement.			**01**

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Semester: IV

Course Title: **Product Realization**	Course Code: 17EECF203
Total Contact Credits: **2** **(0-0-2)**	Duration of SEE Credits: -
ISA Marks: 80	ESA Marks: 20

Week #	Particulars	Template #	Venue
Week 1 **and** **Week 2**	➢ Introduction to Prototyping ➢ Defining- Specifications, Part Drawings, Assembly Drawings, PCB Layout, Wireframe , Pseudocode, BOM, Process Plan, Fabrication and Test Plan Validation ➢ IOT Workshop		Studio Engagement
Week 3	➢ Identifying sub-assemblies (minimum of 3) ➢ Selection of materials for all the parts and joining techniques		Makers Space/
Week 4	➢ Process plan ➢ Identifying the proper machines and tools required for prototyping. ➢ Preparing of raw materials for prototyping. ➢ Plan and procure the bought out parts.		
Week 5	➢ Fabricate the parts for sub assembly 1		
Week 6	➢ Fabricate the parts for sub assembly 2		
Week 7	➢ Fabricate the parts for sub assembly 3		
Week 8	➢ Assemble the sub assemblies and check for interference and functionality		
Week 9	➢ Test the functional prototype using proper identified test methods.		

Text Books (List of books as mentioned in the approved syllabus)

5. Clive L Dym and Patrick Little, "Engineering Design: A Project Based Introduction", John Wiley &Sons
6. Yousef Haik, "Engineering Design Process", Cengage Learning India Private Limited, NewDelhi

Week 10	➢ Analyse the test results ➢ System modification		
Week 11	➢ Final concluding review ➢ Product catalogue		Studio/ Makers Space

References

1. Pahl, G., Beitz, W., Feldhusen, J. and Grote ; "Engineering Design-A Systematic Approach" by, K.-H- Springer; 3rd ed. 2007

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Course Title: **Embedded Intelligent Systems**		Course Code: 17EECE310
L-T-P: 0-0-3	Credits: 3	Contact Hrs: **6hrs/week**
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hrs: 60	Exam Duration: 3 hrs	

	Unit - I	
1	**Basics of embedded systems** Linux Application Programming, System V IPC, . Linux Kernel Internals and Architecture , Kernel Core , Linux Device Driver Programming, Interrupts & Timers , Sample shell script, application program, driver source build and execute	**10 hrs**
2	**Heterogeneous computing** Basics of heterogeneous computing with various hardware architectures designed for specific type of tasks, Advanced heterogeneous computing with a. Introduction to Parallel programming b.GPU programming (OpenCL). Open standards for heterogeneous computing (Openvx) , Basic OpenCL examples - Coding, compilation and execution	**12 hrs**
	Unit - II	
3	**ML Frameworks with the target device** Caffe, tensorflow, TF Lite machine learning frameworks & architecture ,Model parsing, feature support and flexibility ,Supported layers , advantages and disadvantages with each of these frameworks, Android NN architecture overview , Full stack compilation and execution on embedded device	**16 hrs**
4	**Model Development and Optimization** Significance of on device AI ,Quantization , pruning, weight sharing, Distillation ,Various pre-trained networks and design considerations to choose a particular pre-trained model ,Federated Learning , Flexible Inferencing	**8 hrs**
	Unit - III	
5	**Android Anatomy** Android Architecture ,Linux Kernel , Binder , HAL Native Libraries , Android Runtime, Dalvik Application framework , Applications, IPC	**8 hrs**

Text Books

1. Linux System Programming , by Robert Love , Copyright © 2007 O'Reilly Media
2. Heterogeneous Computing with OpenCL, 2nd Edition by Dana Schaa, Perhaad Mistry, David R. Kaeli, Lee Howes, Benedict Gaster , Publisher: Morgan Kaufmann

Reference Books:

1. Deep Learning , MIT Press book ,Goodfellow, Bengio, and Courville's
2. Beginning Android , by Wei-Meng Lee , Publisher: Wrox , O'Reilly Media

Scheme for End Semester Assessment (ESA)

UNIT	Experiments to be set of 10 Marks Each	Chapter Numbers	Instructions
I	Project Examination	1,2,3,4,5	Project implementation and demonstration 20 marks

Laboratory Title: **C Programming (for Diploma)**	Lab. Code:
Total Hours: 20	Duration of Exam: 02
ESA Marks: 20	Total ISA. Marks: 80

Experiment wise plan

1. **List of experiments/jobs planned to meet the requirements of the course.**

Expt./Job No.	Experiment/job Details	No. of Lab. Session/s per batch (estimate)	Marks/Experiment
1.	Write a C program to perform addition , subtraction , multiplication and division of two numbers .	01	8.00
2.	Write a C program to i) Identify greater number between two numbers using C program. ii) To check a given number is Even or Odd .	01	8.00
3.	Write a C program to i) To find the roots of a quadratic equation. ii) Find the factorial of given number.	01	8.00
4.	Write a C program to i) To find the sum of n natural numbers. ii) Print the sum of 1 + 3 + 5 + 7 + + n	01	8.00
5.	Write a C program to i) Print the pattern . * * * * * * * * * * * * * * * ii) Print the pattern 1 1 2 1 2 3 1 2 3 4 1 2 3 4 5	01	8.00

6.	Write a C program to To test whether the given character is Vowel or not. (using switch case)	01	8.00
7.	Write a C program to To accept 10 numbers and make the average of the numbers using one dimensional array.	01	8.00
8.	Write a C program to Find out square of a number using function.	01	8.00
9	Write a C program to To find the summation of three numbers using function.	01	8.00
10	Write a C program to Find out addition of two matrices.	01	8.00

1. **Materials and Resources Required:**

Text Book

1. Programming in ANSI C, E Balagurusamy

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)			**Lab+ Teaching Hours**
Course Title: Data Structures Application Lab		**Course Code: 18EECC210**	
L-T-P: 0-0-2	**Credits: 2**	**Contact Hours: 4Hrs/week**	
ISA Marks: 80	**ESA Marks:20**	**Total Marks: 100**	
Teaching + Lab. Hours: 48 Hrs	**Examination Duration:2 Hrs**		

1.	**Hashing** Hash, Hash function, Hash Table, Collision resolution techniques, Hashing Applications	12Hrs
2.	**Trees** Computer representation, Tree properties, Binary Tree properties, Binary search trees properties and implementation, Tree traversals, AVL tree, 2-3 Tree	20Hrs
3.	**Graphs** Computer representation, Adjacency List, Adjacency Matrix, Graph properties, Graph traversals	16Hrs

Book

1. Data Structures A Psedocode Approach with C, Richard F. Gilberg & Behrouz A. Forouzan, second edition, CENGAGE Learning.

2. Data Structures Using C. Author, Aaron M. Tenenbaum. Publisher, Pearson Education.

Course Title: **CMOS ASIC Design**	Course code: 18EECE420	
L-T- P: 0-0-3	Credits: 03	Contact Hrs: 06hrs/week
CIE Marks: 100	SEE Marks: 00	Total Marks: 100
Teaching Hrs: 16hrs Lab Hrs: 24 hrs		

Chapter No. 1. Introduction: Design of combinational and sequential logic gates in CMOS. Layout and characterization of standard cells. Verilog for representing gate level netlists.	8 hrs
Chapter No. 2. Timing Analysis: Sequential circuit timing and static timing analysis. Cell and net delays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock Domains	10hrs
Chapter No. 3: Physical design Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew.	12 hrs
Chapter No. 4. Standard Data formats: Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes.	6 hrs
Chapter No. 5. Packaging An overview of package design and implementation and system level timing.	4 hrs

Reference Books:

1. The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985.
2. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime, 2nd edition, 2001.
3. Static Timing Analysis for Nanometer Designs A Practical Approach, J. Bhasker • Rakesh Chadha, Springer Science+Business Media, LLC 2009

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Course Title: **Physical Design-Analog**	Course code: 18EECE419	
L-T- P: 0-0-3	Credits: 03	Contact Hrs: 06hrs/week
CIE Marks: 100	SEE Marks: 00	Total Marks: 100
Teaching Hrs: 16hrs Lab Hrs: 24 hrs		

Chapter No 1. Standard cell Layout creation Layout Practice Sessions (DRC/LVS Dirty layout), Understanding verification errors, Error debugging skills, Hands on experience of using layout editor, Quality of the layout, Half DRC rules, Mega module creation.	8 hrs
Chapter No 2. Analog layout Importance of performance in Analog layout, Importance of floor planning and placement, Attributes need to be taken care during routing stage, Introduction to DRC, LVS, Density and RCX.	8 hrs
Chapter No 3. Matching and Guard rings, Matching: Introduction to mismatch concepts, Causes for mismatch, Types of mismatch, Rules for matching, Activities. Guard ring : What is guard ring, Usage of guard ring	6 hrs
Chapter No 4. Reliability issues Introduction to failure mechanism, Causes of reliability issues, Process enhancement techniques and Layout considerations to reduce reliability issues	8 hrs
Chapter No 5. Physical design of amplifier and buffer Applying the studied concepts and doing layout, Prioritising the constraints given, Quality checks, Buddy reviews and implementations, Documentation	10 hrs

Reference:

The Art of Analog Layout – Alan Hastings

CMOS IC layout – Dan Clien

IC Layout Basics – Chris saint and Judy saint

Course Code: **19EECE322 / 19EECE422**	Course Title: **Introduction to Deep Learning**	
L-T-P: **2-0-1**	Credits: **3**	Contact Hrs: **4**
ISA Marks: **50**	ESA Marks: **50**	Total Marks: **100**
Teaching Hrs: **42**		Exam Duration: **3 hrs**

Content	**Hrs**
Unit - 1	
Chapter 1: Introduction to Deep Learning: What is Deep Learning?, Applications of deep learning, Differences between machine learningand deep learning, Basics of Neural Networks, Supervised Learning with Neural Networks, Logistic regression as a neural network, Computation graph, shallow neural networks, Deep neural networks. Introduction to metric tensors and tensorflow, Basic programs in tensorflow.	8 hrs
Chapter 2: Hyper-Parameter Tuning, Regularization and Optimization: Basics of Hyper-parameters, Regularization, Need for regularization, dropout regularization, gradient checking, mini-batch gradient descent, exponentially weighted averages and its biascorrection, Gradient descent with decay, Adam's optimization algorithm, The problem of localminima, weight initialization in neural networks, Normalizing activations in a network, Fitting Batch norm into a network, Softmax regression, Softmax classifier.	8 hrs
Unit - 2	
Chapter 3: Convolutional Neural Networks Introduction to Computer Vision and Image Processing, 2D Convolutions, Strided convolution,convolution over volume, One layer of a convolution network, ReLu and pooling, Example of aConvNet, Classic CNN Networks, ResNet architecture, Inception Networks, Transfer learning,Data Augmentation, Residual networks, Object Localization, Landmark and object detection, Convolutional implementation of sliding windows, YOLO algorithm, Car detection algorithm using YOLO, One shot learning, Face recognition algorithm.	12 hrs
Chapter 4: Recurrent Neural Networks Backpropogation through time, RNN model, Types of RNN, Vanishing gradients with RNN,Gated Recurrent Unit, LSTM, Bidirectional RNN, Deep RNN, basics of NLP and Concept ofword embedding, speech recognition.	04 hrs
Unit - 3	
Chapter 5: Unsupervised Deep Learning Concepts of Unsupervised deep learning, RBM (Restricted Boltzman Machine) and auto encoders, structure of Auto encoders, collaborative filtering with RBM, Deep belief networks.	10 hrs

Text Books

- Deep Learning, Ian Goodfellow, Yoshua Bengio and Aaron Courville, MIT Press, http://www.deeplearningbook.org, 2016.
- Neural Networks and Deep Learning by Michael Nielsen.

References

- Deep Learning with Python, Francois Chollet, by Manning Publications, 2018.
- Deep Learning by Microsoft Research
- Deep Learning Tutorial by LISA lab, University of Montreal

Laboratory Title: **Senior Design Project**	Lab. Code:**20EECW401**
Credit : 0-0-6 Total Hours: 70**hours/week**	Duration of exam: **2 hours**
Total Exam Marks: **100**	ISA Marks: **50**

Application Areas are,

- Smart City
- Connected Cars
- Home Automation
- Health care
- Smart energy
- Automation of Agriculture

Guide lines for selection of a project:

- The project needs to encompass the concepts learnt in the previous semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the defined problem statement of the project work.
- Student can select a project which leads to a product or model or prototype.
- Time plan: Effort to do the project should be between 60-70Hrs per team, which includes self-study of an individual member (80-100 Hrs) and team work (40-50hrs).
- Learning overhead should be 20-25% of total project development time.

Criteria for group formation:

- 3-4 students in a team.
- Role of teammates: Team lead and members.

Allocation of Guides and Mentors for the projects:

Every Project batch will be allocated with one faculty.

Details of the project batches:

- Number of faculty - members: 50
- Number of students:3-4 students in a team.

Role of a Guide

The primary responsibility of the guide is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, guide should help towards its successful completion as per the predefined standards.

How student should carry out a project:

- Define the problem.
- Specify the requirements.
- Specify the design in the understandable form (Block Diagram, Flowchart,Algorithm,etc).
- Analyze the design and identify hardware and software componentsseparately.
- Select appropriate simulation tool and development board for the design.
- Implement the design.
- Optimize the design and generate the results.
- Result representation and analysis.
- Prepare a document and presentation.

Report Writing

- The format for report writing should be downloaded from ftp://10.3.0.3/projects
- The report needs to be shown to guide and committee for each review.
-

Evaluation Scheme

- Internal semester assessment (ISA)
- Evaluation is done based on the evaluation rubrics given in Table 1
- Project shall be reviewed and evaluated by the concerned Guide for 50% of the marks.
- Project shall be evaluated by the review committeefor 50% of the marks.

Course Code: 20EECE406	Course Title: AUTOSAR	
L-T-P: 3-0-0	Credits: 3	Contact Hrs: 40
CIA Marks: 50	SEE Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3 hrs

Content	Hrs
Unit - 1	
Chapter No. 1: AUTOSAR Fundamentals Evolution of AUTOSAR – Motivations and Objectives AUTOSAR consortium – Stake holders – work Packages, AUTOSAR Partnership, Goals of the partnership, Organization of the partnership, AUTOSAR specification, AUTOSAR Current development status, BSW Conformance classes: ICC1, ICC2, ICC3, and Drawbacks of AUTOSAR.	8 hrs
Chapter No. 2: AUTOSAR layered Architecture AUTOSAR Basic software, Details on the various layers , Details on the stacks Virtual Function Bus (VFB) Concept Overview of AUTOSAR Methodology , Tools and Technologies for AUTOSAR AUTOSAR Application Software Component (SW-C) ,Types of SW-components AUTOSAR Run Time Environment (RTE): RTE Generation Process: Contract Phase, Generation Phase, MCAL, IO HW Abstraction Layer, Partial Networking, Multicore, J1939 Overview, AUTOSAR Ethernet, AUTOSAR E2E Overview , AUTOSAR XCP, Metamodel , From the model to the process , Software development process.	7 hrs
Unit - 2	
Chapter No. 3: Methodology of AUTOSAR and Communication in AUTOSAR CAN Communication, CAN FD, CANape, Application Layer and RTE, intra and inter ECU communication, Client-Server Communication, Sender-Receiver, Communication, CAN Driver, Communication Manager (ComM), Overview of Diagnostics Event and Communication Manager	10 hrs
Chapter No. 4: Overview about BSW constituents BSW Constituents: Memory layer, COM and Services layer, ECU abstraction, AUTOSAR, Operating system, Interfaces: Standard interface, AUTOSAR standardized interface, BSW-RTE interface,(AUTOSAR interface), BSW-ECU hardware interface, Complex device drivers and BSW module configuration, AUTOSAR Integration.	5 hrs
Unit - 3	
Chapter 5: MCAL and ECU abstraction Layer Microcontroller Drivers, Memory drivers: on-chip and off chip drivers, IO drivers(ADC, PWM, DIO), Communication drivers: CAN driver, LIN drivers, Flexrfay	5 hrs
Chapter 6: Service Layer	5 hrs

Diagnostic Event Manager, Function inhibits Manager, Diagnostic communication manager, Network management, Protocol data unit router, Diagnostic log and trace unit, COMM manager.	

Text Books (List of books as mentioned in the approved syllabus)

Ronald K. Jurgen, Infotainment systems, 2007, SAE International, 2007

Laboratory Title: **Project Work**	Lab. Code:**20EECW402**
Credit : 0-0-11 Total Hours: **22 hours/week**	Duration of exam: 2
Total Exam Marks: ISA : 50	ESA Marks: **50**

Application Areas are,

- Smart City
- Connected Cars
- Home Automation
- Health care
- Smart energy
- Automation of Agriculture

Guide lines for selection of a project:

- The project needs to encompass the concepts leant in a subject/s studied in the previous seven semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the defined problem statement of the project work.
- Student can select a project which leads to a product or model or prototype.
- Time plan: Effort to do the project should be between 120-150 Hrs per team, which includes self-study of an individual member (80-100 Hrs) and team work (40-50hrs).
- Learning overhead should be 20-25% of total project development time.

Criteria for group formation:

- 3-4 students in a team.
- Role of teammates: Team lead and members.

Allocation of Guides and Mentors for the projects:

Every Project batch will be allocated with one faculty.

Details of the project batches:

- Number of faculty members : 64
- Number of students:3-4 students in a team-46 Teams
- Internship Students:93

Role of a Guide

The primary responsibility of the guide is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, guide should help towards its successful completion as per the predefined standards.

How student should carry out a project:

- Define the problem
- Specify the requirements
- Specify the design in the understandable form (Block Diagram, Flowchart,Algorithm,etc)
- Analyze the design with hardware and software components saparately.
- Select appropriate simulation tool and development board for the design.
- Implement the design
- Optimize the design and generate the results
- Result representation and analysis
- Prepare a document and presentation.

Report Writing

- The format for report writing should be downloaded from ftp://10.3.0.3/projects
- The report needs to be shown to guide and committee for each review.

Evaluation Scheme

Internal semester assessment (ISA)

Evaluation is done based on the evaluation rubrics given in Table 1

- Project shall be reviewed and evaluated by the concerned Guide for 50% of the marks.
- Project shall be evaluated by the review committee for 50% of the marks.

Course Title: Internship- Project	Course Code: 20EECW494
L-T-P: 0-0-11	Duration of ESA: 2hr
ESA Marks: 50	ISA Marks: 50

Engineering graduates unlike graduates from other fields require a strong industry connect during the course. This experience is provided through industry internships during VIII Semester of the program. Internships make students more competitive in the job market. During internship the student gains competency while working on live projects meeting all the deadlines related to project work. The students of the VIII semester are permitted to opt for full-time Industry Internship. Students having placement offers usually undergo internship at their respective industries, while others choose industry, based on their competency in consultation with the department.

The implementation details and impact of internships in the department are discussed below.

The internship has 2 mandatory components; i) Internship Training, and ii) Internship – Project.

- Internship Training: Industry offers training in learning tools/ framework / programming language / Industrial practices to carry out the Internship project.
- Internship-Project: Industry assigns a well-defined problem statement for the project and provides an industry mentor to execute the project. The University guide in consultation with Industry Guide reviews the project progress at regular intervals using Skype/ Webex or personal visit to the industry.

At the end of the Internship, student has to submit Internship Training Report & Internship Project report to the University. Contents of the Reports shall be decided in consultation with Industry Guide. Industry shall issue Internship Certificate to student-intern.

The expectations from most of the problem statements were either to develop a subsystem of a bigger system or development of a relatively smaller system itself. Students developed either a working prototype or proof of concept as part of their project work. Students worked on simulation projects as well.