KLE Technological University Mail

Saroja V. Siddamal <sarojavs@kletech.ac.in>

schedule for 9th june

2 messages

Saroja V.S. . <sarojavs@bvb.edu> Tue, Jun 5, 2018 at 11:04 AM
To: Anand Bariya <bariya@gmail.com>

Sir

Will you talk about packaging.
Is this schedule ok for you

SL.No		TIME	Members present
1	Class on Packaging	9:00 am to 10:45	All Students
2	Power reduction in chain Scan insertion discussion --REU	11:00 to 12:00	Saroja+ Harshaverdan
3	Project Discussion	12:00 to 1:00	Srripad + Anand+ faculty
4	Functional final review of Mixed signal IC	2:30 to 4:30	All students (analog+digital) Mentors+ faculty

I have spoken to Manjunath if he comes then we can run the complete flow for Mixed signal IC .

Regards
Saroja

Anand Bariya <bariya@gmail.com> Tue, Jun 5, 2018 at 12:03 PM
To: "Saroja V.S. ." <sarojavs@bvb.edu>

Saroja,

Sounds good.

I will need some time to meet with Shettar-sir to discuss future activities. Vivek is organizing. But that should not be a problem. I will target for 4:30.

Also, I need to go to Goa from Hubli, and not return to Bangalore. Can you please book on the usual Hubli-Vasco train for Saturday night?

- Anand
[Quoted text hidden]

Visit of Dr. Anand Bariya–August 2018 to July 2019

Date	Schedule	Content covered	Contact Hrs
6/8/2018	10:00am to 1:00am	Discussion with Mentor Graphics	7
	2:00 am to 3:00 am	Review of NKETC project	
	3:00 am to 6:00 am	Flow development.	
7/8/2018	10:00am to 1:00am	ASIC Class	7
	2:00 am to 3:00 am	PDK Project Discussion	
	3:00 am to 6:00 am	NKETC Progress	
1/09/2018	10:00am to 1:00am	scan insertion, placement, clock tree synthesis and routing.	7
	2:00 am to 3:00 am	Netlist transformations	
	3:00 am to 6:00 am	Project Review	
22/09/2019	10:00am to 1:00am	Net parasitic and parasitic extraction. Use of PLLs for clock generation and clock skew	7
	2:00 am to 3:00 am	Standard data formats	
	3:00 am to 6:00 am	Clock gating and power gating	
22/10/2018	10:00 am to 12:00am	Discussion on NKETC Sign off	7
	12:00 am to 1:00 am	Recruitment Test	
	2:00 am to 4:00 am	Interview	
	3:00 am to 6:00 am	Selection	
2/2/2019	10:00 am to 1:00 am	Static Time Analysis	7
	2:00 am to 3:00 am	PDK development	
	3:00 am to 6:00 am	Chip Design	
16/2/2019	9::00 am to 11:00am	Discussion on this year's and five years plan.	
	11:00 am to 12:00am	PDK Development	
	12:00 am to 1:00am	Meeting With VC sir	
	1:30 am to 6:30 am	CMOS ASIC Class –STA	
17/2/2019	10:00 am to 12:00am	CMOS ASIC Class –STA	8
	12:00 pm to 1:00pm	Opportunities in VLSI	

		industries	
	1:30 am to 6:30 am	CMOS ASIC Class	
23/2/2019	10:00 am to 1:00 am	CMOS ASIC Class –Tempus-TA	7
	2:00 am to 6:00 am	PDK development	
16/3/2019	10:00 am to 12:00am	Design for reliability	7
	12:15 pm to 2:00pm	Overview of package design	
	2:30 pm to 5:30pm	Project Review	
22/4/2019	9:00 am to 9:30 am	SRAM instantiation	8
	9:30 am to 10:00 am	Discussion on Chisel	
	10:00 am to 11:00am	Discussion on Event logger + Testing of NKETC	
	11:00 am to 12:30am	Class	
	12:30 am to 1:30 am	Lunch	
	1:30 am to 2:30 am	RISC V	
	2:30 am to 6:00 am	Discussion on Chisel	
18/5/2019	10:00 am to 1:00 am	CMOS ASIC Class –Voltas	6
	2:00 am to 5:00 am	PDK development Review	
08/6/2019	10:00 am to 12:00am	CMOS ASIC Class	6
	12:15 pm to 2:00pm	Project Review	
	2:30 pm to 4:30pm	Discussion on Event logger + Testing of NKETC	
09/6/2019	9:30 am to 12:00am	CMOS ASIC Class	7
	12:15 pm to 1:30pm	Process development discussion	
	2:00pm to 5:00pm	Further discussion on NKEL2020	
13/7/2019	9:30 am to 12:00 am	P&R Flow	7
	12:15 pm to 1:30pm	Discussion on Chisel	
	2:00pm to 5:00pm	Review of NKEL2020	

Total no of contact Hrs: 98

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Visit of Dr. Anand Bariya August 2019-July 2020

Date	Schedule	Content covered	Contact Hrs
8/8/2019	9:00 to 6:00	Chisel boot Camp	9
9/8/2019	9:00 to 6:00	Chisel boot Camp	9
9/8/2019	9:00 to 6:00	Chisel boot Camp	9
10/9/2019	10:00 to 12:30	Formats Class	7
	12:30 to 1:30	Discussion on nest year project	
	2:30 to 6:00	Chip design project review	
19/10/2020	10:00 to 12:30	Timing Analysis Class	7
	12:30 to 1:30	Discussion on selection Process	
	2:30 to 6:00	Chip design project review	
25/11/2019	10:00 to 12:30	IO and Packaging	6
	1:30 to 5:00	Selection for Si-Five	
21/12/2019	10:00 to 12:30	Chip design project review	7
	1:30 to 6:00	Discussion on Next year project	
Total no of contact Hrs: 50			

Visit of Shripad Annigeri August 2018-July 2019

Date	Schedule	Content covered	Contact Hrs
21/8/18	9:30-10:30	In the lab to check IO Library for X1/X2 crystal oscillator pins.	7
	10:30 to 11:15	With IO team members on cut cell layout modification discussion.	
	11:30 to 12:00	Chip top verilog netlist discussion (bi directional data pin).	
	12:00 to 12:30	IO ring discussion with cut cell and oscillator cells (IO team and chip top team)	
	1:30-5:30	BGR Layout review and issues related to LEF generation	
5/9/18	9:30 to 10:30	Calibre drc run on one layout (may be oscillator) : In the lab : 1 hour	6
	10:30-11:00	Shuttle booking and pending activities for tapeout.	
	11:00 to 11:30	REU : Elapsed Time counter	
	11:30 to 12:30	REU Discussion: Diff VCO design.	
	1:30 to 2:00	UVLO Architecture Discussiom	
	2:00 to 4:30		
6/9/18	9:00 to 10:30	Finalisation of IO Ring	6
	10:30 to 11:00	Re check on correct IO library — 3.3V, 6 Metal, No pad on active area library —MM RF and GII Logic	
	11:00 to 11:30	Identify Pad cell and usage of that at chip top	
	11:30 to 12:30	Layout check of UVLO and IO cell	
	1:30 to 2:00	final design doc check	
	2:00 to 4:00	Next batch activities	
21/9/18	10;00 to 12;30	Review of Oscillator and Comparator	6
22/9/18	10;00 to 12;30	Review of NKETC, tap out	
25/10/18	10:00 to 4;00	Chip tape out	
12/12/18	10:00am-11:30am	Patent discussion Remaining activities of NKETC2019 design	
	11:30am-1:00am	Plan for data management changes, data security steps and tool/pdk re-installation	
	3:00pm- 4:00pm	Concrete plan for coming year (2019) Discussion with Resource person on Logic Verification course — Naveen Desai.	
	4:00pm- 6:00pm	Analog discussion - PhD students	
13/12/2018			
	9:00am-10:30am	Discussion on 5 year plan	9

	10:30am-12:30am	Analog activities for mixed signal chip. Other blocks/designs Discussion on Selection of students for next batch	
	12:30 to 1:00	Discussion on PLL	
	2:00 to 3:00	Discussion on LDO	
	3:00 to 4:00	Discussion on Event logger	
	4:00 to 6:00		
29/1/2019	10:00 to 11:30	Presentation of DS1683 by Chip design Students and discussion	
	11:30 to 12:00	Address students on how IMEC shuttles are manufactured –Shripad	8
	12:30 to 1:00	Final Presentation by REU student (VCO) Pranav Kulkarni	
	2:00 to 3:00	Updates from Analog Chip design Teams, Discussion on OSC and LDO	
	3:00 to 4:00	Test plan of oscillator and UVLO in NKETC2019 Reference document is data sheet of NKETC2019—Shraddha	
	4:00 to 6:00	Microprocessor development project Presentation by teams	
15/2/2019	10:00 to 11:00	Discussion on spec of 1683 and name of this chip	
	11:00 to 12:00	Test plan of NKETC2019 Execution plan of this year's project Power on Reset and configuring all register to some default sets. Verilog wrapper for analog blocks to store configure bits (e.g. trim bits) and the same can be read back by top level status register (through I2C).	7
	12:00 to 12:30	Oscillator patent next step	
	12:30 to 1:30	Analog block progress : Simulation of Osc and UVLO of NKETC2019	
	3:00 to 4:00	ARM M0/M3 micro processor	
	4:00 to 6:00	Osc and LDO Teams	
16/2/2019	9:30 to 11:00	Discussion on this year's and five years plan.	3
	11:00 to 12:00	PDK Development With Anand Sir	
	11:00 to 12:00	Status on SVN repository	
	12:00 to 12:30	Meeting with VC sir	
6/3/2019			
	9:30 to 10:30	Functional Description of the chip a. First cut feature and function presentation and inviting feedback, comment and any extra features	2

		from students and faculty.—All	
	10:30 to 11:00	Brief presentation on ASIC design project mile stones-Shripad	
	11:00 to 11:30	Design spec development role distribution—	
7/3/2019			
	9:30 to 10:00	Ring oscillator basics : A lecture —Shripad	3
	10:0 0 to 11:00	Status check of LDO block —Sujatha	
	11:00 to 12:30	Patent next stage	
8/3/2019			
	10:00 to 10:30	Testing of NKETC — test plan document and test board verification status --Suhas	5
	10:30 to 11:15	TRNG—Saroja	
	11:15 to 12:00	555 timer—Sujatha	
	12:00 to 12:45	IO and std cell library development proposal Processor study and developing our own small processor	
	1:30 to 4:00	ARM M0/M3 Processor hardening status discussion.	
22/4/2019	10:00 to 11:00	Discussion on Event logger + Testing of NKETC	6
	11:00 to 12:30	Oscillator	
	1:30 to 2:30	LDO	
	2:30 to 3:30	Microprocessor development for ASIC	
	3:30 to 5:00	Patent Discussion	
12/6/19	10.00 to 12:00	Review of oscillator design	7
	12:00 to 1:00	TSMC 180nm PDK installation check and handing over to students.	
	2:00 to 4:00	NKETC 2019 Testing	
	4:00 to 6:00	Oscillator patent submission	
13/6/19	10:30 to 12:00	Talk on “Passive devices in Ics”	6
	12:00 to 1:00	Overall 2020 chip design progress and plan alignment	
	2:00 to 3:30	Progress updates of LDO	
	3:30 to 5:30	Any other discussion	
25/6/2019			
	10:00 to 11:00	Review of cut overlap cell gds of NKETC2019 to check any short.	5
	11:00 to 12:00	Review of NKETC power supply short and further action.()	
	12:00 to 1:00	Update of LDO, Oscillator and other analog block design from faculty — (respective faculty members can review the design before and get design/status details).	

	2:00 to 4:00	Study of TSMC IO cells	
26/6/2016			
	10:00 to 11:00	Presentation by Shripad : ESD overview	2
	11:00 to 12:00	Discussion with Oscillator design team.	
10/7/2019			
	10:00 to 11:00	Simulation of NK*2020	
	11:00 to 11:30	NK*2020 Project progress discussion	7
	11:30 to 12:30	NKETC2019 Debug discussion.	
	1:30 to 2:30	NK*2020 Analog macro spec review — Oscillator	
	2:30 to 6:00	TSMC PDK Issues	
11/7/2019			
	10:00 to 11:00	TRNG	6
	11:00 to 12:00	NK*2020 Analog macro spec review — LDO	
	12:00 to 1:00	Review of POR	
	2:00 to 5:00	Back end report	

Total No of Contact Hrs: 103

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Visit of Shripad Annigeri August 2019-July 2020

Date	Schedule	Content covered	Contact Hrs
6/8/19	10:00 to 11:00	NKETC2019 Failure analysis and further steps	5
	11:00 to 12:00	NKEL2020 TSMC design kit Memory, Calibra etc	
	12:00 to 1:00	Oscillator design review	
	2:00 to 3:00	Simulation of NK*2020" with digital team. Pin finalization	
7/8/19	10:00 to 11:00	Prakalp team (5^{th} sem) — technical interaction	6
	11:00 to 1:00	Brief update on LDO+ other analog block progress.	
	2:00 to 3:00	Discussion on packaging — next year silicon — Tessolve or other companies	
	3:00 to 4:00	Placement and connecting with industry.	
27/8/19	10:00 to 11:00	Pinout freezing for 2020 product	3
	11:00 to 12:00	Oscillator review	
	12:00 to 1:00	Interaction with Prakalp students	
28/8/19	10:00 to 11:00	Review of IO excel sheet	4
	11:00 to 12:00	Failure analysis of NKETC2019	
	12:00 to 12:30	Updates of LDO	
17/9/19	10:00 to 11:00	Layout mitigation-Ekalakshya	6
	11:00 to 12:00	Pin out and IO ring discussions	
	12:00 to 1:00	Clarifications from IMEC+ Lef issues+ calibre	
	2:00 to 3:00	Memory instances	
	3:00 to 4:00	LDO Review design progress using design doc, (showing waveform/schematic etc).	
18/9/19	10:00 to 11:00	Oscillator Review design progress using design doc, (showing waveform/schematic etc).	2
	11:00 to 12:00	NKETC 2019- LVS	
15/10/2019			
	10:00 to 11:00	Current chip design progress and issues	6
	11:00 to 12:00	Analog macro-Oscillator + LDO update (Trim bit register, final pinout etc)	
	12:00 to 1:00	IO discussion, pinout, final block dig, analog trim bit issues	
	2:30 to 3:00pm	PLL and DC/DC update	
	3:00 to 4pm	Next Year Project and industry support	
16/10/2019			
	10:00 to 11:00	LVS of last ETC2019	6
	11:00 to 12:00	Testing of Last ETC2019	
	12:00 to 1:00	SCL PDK any update and future activities	

	2:00 to 3:00	Learning from VSD training on freeware based SoC design. Can we try it next year on one design.	
	3:00 to 4:00	Logic verification for current project.	
14/12/2019	10:00 to 12:00	GDS of chip top, DRC	7
	12:00 to 1:00	Discussion on LDO , OSC	
	2:00 to 3:00	Next year Plan	
	3:00 to 4:00	DC-DC and LDO	
	4:00 to 4:30	IO Design Discussion	
	4:30 to 5:00	TRNG	
11/1/2020	10:00 to 10:30	Discussion with HoS –Course	6
	10:30 to 11:00	Advanced SoC development course introduction to students	
	11:00 to 11:30	EL 2020 Updates	
	11:30 to 1:00	Next year chip design activities plan.	
	1:00 to 1:30	Lunch	
	1:30 to 2:00	Next year Analog block development plan/proposal	
	2:00 to 2:30	TRNG Circuit project — NIST tool progress	
	2:30 to 3:00	Meeting with Desai Sir	

Total No of contact Hrs: 53