KLE Technological University
Creating Value Leveraging Knowledge

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING

Computer Organization & Architecture Lab (18ECSP202)

(2019-20)

1. Course Outcomes-CO

At the end of the course students will be able to:

i. Design and implement combinational and sequential circuits.
ii. Design and implement basic computer building blocks.
iii. Simulate computer building blocks using a suitable tool

Course Articulation Matrix: Mapping of Course Outcomes (CO) Program outcomes

Course Title: **Computer Organization and Architecture** Course code: **18ECSP202** Semester: **III** Year: **2019-20**

Course outcomes-CO/Program Outcomes-PO	**1**	**2**	**3**	**4**	**5**		**6**	**7**	**8**	**9**	**10**	**11**	**12**
1. Design and implement combinational and sequential circuits.	H		M		M								
2. Design and implement basic computer building blocks.	H		M		M								
3. Design & simulate computer building blocks using a suitable tool.		H	H		H					M	M		

Degree of compliance **L**: Low **M**: Medium **H**: High

2. Experiment list

1. List of experiments/jobs planned to meet the requirements of the course.

Category: Exercises	*Total Weightage: 60*	*No. of lab sessions: 08*		
Learning Outcomes: *The students should be able to:* 1. *Demonstrates the usage of Digital trainer kit.* 2. *Design and implement basic Combinational circuits.* 3. *Design and implement computer building blocks.*				
Expt./Job No.	***Experiment/job Details***	***No. of Lab. Session/s per batch (estimate)***	***Marks/Experiment***	***Correlation of Experiment with the theory***
1	Design, implement and simulate basic combinational circuits.	01	30 marks	Chapter 1 & 2
2.	Design, implement and simulate Ripple Carry Adders	01		
3.	Design, implement and simulate Carry-Look-Ahead Adder	02		
4.	Design, implement and simulate 1-bit ALU	01	30 marks	
5.	Design, implement and simulate counters	01		
6.	Design, implement and simulate simple memory modules	02		Chapter 3 & 4
Category: Structured Enquiry	***Total Weightage: 20***	***No. of lab sessions: 04***		
Learning Outcomes : *The students should be able to:* 1. *Design and simulate computer building blocks using a suitable tool.*				
Expt./Job No.	***Experiment/job Details***	***No. of Lab. Session/s per batch (estimate)***	***Marks/ Experiment***	***Correlation of Experiment with the theory***
1.	Study and analyze datapath/module design of Data transfer, arithmetic and branch instructions using appropriate tool	4	15 marks	Chapter 2

3. Rubrics for Assessment

a. Rubrics for ISA (80M)

Assessment	Criteria	Excellent	Good	Average	PI
Combinational Circuit design (30M)	Design (5M)	Student is able to: 1. Select appropriate input & output variables. 2. Use K-map to obtain minimal expression. 3. Draw logic diagram for minimal expression. (5M)	Student is able to: 1. Select appropriate input & output variables. 2. Use K-map to obtain minimal expression. (2-4M)	Student is able to: 1. Select appropriate input & output variables. (0-1M)	1.4.4 3.3.1 5.3.1
	Conduction (10M)	1. Proper selection of component is done. 2. Testing of Components and Equipments to be done. 3. Circuit connections are done using appropriate number of patch chords so that tracing circuit is becomes easier. 4. Circuit and power supply connections are appropriate. (8-10M)	Selection of components is improper / verification of components for proper working is not done/Un identification of input and outputs for used ICs / improper circuit connections. (4-7M)	Lack of knowledge about components or connections. (0-3M)	
	Simulation (10M)	Able to simulate designed circuit and the simulation shows output for all possible inputs. (8-10M)	Unable to simulate the circuit properly and hence the simulation is partial. (3-7M)	Unable to simulate the circuit. (0-2M)	
	Viva (5M)	Student will be able to answer 100% of the questions based on combinational circuits. (4-5m)	Student will be able to answer above 50% of the questions based on	1. Student will be able to answer below 50% of the questions	

			combinational circuits (2-3M)	based on combinational circuits 2. (0-1M)	
Sequential Circuit design (30M)	Design (5M)	Student is able to: 1. Select appropriate of input output variables. 2. Use appropriate flip-flops and other gates to design sequential circuits. 3. Draw logic diagram for minimal expression. (5M)	Student is able to 1. Select appropriate of input output variables. 2. Use appropriate flip-flops and other gates to design sequential circuits. (2-4M)	Student is able to 1. Select appropriate of input output variables. (0-1M)	1.4.4 3.3.1 5.3.1
	Conduction (10M)	1. Proper selection of component is done. 2. Testing of Components and Equipments to be done. 3. Circuit connections are done using appropriate number of patch chords so that tracing circuit is becomes easier. 4. Circuit and power supply connections are appropriate. (8-10M)	Selection of components is improper / verification of components for proper working is not done/Un identification of input and outputs for used ICs / improper circuit connections. (4-7M)	Lack of knowledge about components or connections. (0-3M)	
	Simulation (10M)	Able to simulate designed circuit and the simulation shows output for all possible inputs. (8-10M)	Unable to simulate the circuit properly and hence the simulation is partial. (3-7M)	Unable to simulate the circuit. (0-2M)	
	Viva (5M)	Student will be able to answer 100% of the questions based on sequential circuits. (4-5m)	Student will be able to answer above 50% of the questions based on sequential circuits (2-3M)	3. Student will be able to answer below 50% of the questions based on sequential circuits 4. (0-1M)	

Structured Enquiry (20M)	Tool Survey (2M)	Able to survey all the available tools and choose an appropriate one. (2M)	Able to survey, but unable to choose an appropriate tool. (1M)	5. Unable to survey. (0M)	1.4.4 2.1.2 3.3.1 5.3.1 9.2.1 10.2.2
	Data Path Design (4M)	Able to design data path for the given instruction and show output for all possible inputs. (3-4M)	Able to design datapath, but works for only few inputs. (1-2M)	6. Unable to design. (0M)	
	Individual Contribution (3M)	Actively participates as an individual and in a team for successful completion of structured enquiry. (2-3M)	Poor participation in a team. (1M)	7. Doesn't participate in a team. (0M)	
	Innovation (2M)	Able to solve the problem with innovative ideas and arrive at appropriate conclusion. (2M)	Able to solve the problem by adopting the existing methods. (1M)	8. Unable to solve the problem even with existing methods. (0M)	
	Simulation (4M)	Able to simulate designed circuit and the simulation shows output for all possible inputs. (3-4M)	Unable to simulate the circuit properly and hence the simulation is partial. (1-2M)	Unable to simulate the circuit. (0M)	
	Punctuality (5M)	Student has attendance of 95% and above and has maintained lab book neatly with all records. (4-5M)	Student has attendance from 70% to 94% and has lab record which is not upto expected level. (2-3M)	9. Poor attendance and incomplete lab record book. (0-1M).	

b. Rubrics for ESA (20M)

Criteria	**Excellent**	**Good**	**Average**	**PIs**
Design (5M)	Student is able to: 1. Select appropriate input & output variables. 2. Use appropriate digital component to design. 3. Logic diagram drawn for minimal expression is accurate. (4-5M)	Student is able to: 1. Select appropriate input & output variables. 2. Use appropriate digital component to design. (2-3M)	Student is able to: 1. Select appropriate input & output variables. . (0-1M).	1.4.4 3.3.1 5.3.1
Viva (5M)	Student will be able to answer 100% of the questions based on Digital & COA concepts. (4-5m)	Student will be able to answer above 50% of the questions based on Digital & COA concepts (2-3M)	Student will be able to answer below 50% of the questions based on Digital & COA concepts. (0-1M)	
Component selection ,Connections & Execution (10M).	1. Circuit and power supply connections are appropriate. 2. Testing of Components and Equipments is done. 3. For different components like MUX, Decoder, Flip-flops identification of inputs and outputs is known. 4. Conduction is done within allotted time. 5. Modifications asked to current experiment are done. (8-10M)	Selection of components is improper / verification of components for proper working is not done/Un identification of input and outputs for used ICs / improper circuit connections./Unable to show the conduction within time. (4-7M)	Lack of knowledge about components or connections. (0-3M)	

4. Planning & Attainment

a. Course Assessment Plan

Course Name	CO's	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10
18ECSP202.1	Design and implement combinational and sequential circuits.	3	-	2	-	2	-	-	-	-	-
18ECSP202.2	Design and implement basic computer building blocks.	3	-	2	-	2	-	-	-	-	-
18ECSP202.3	Simulate computer building blocks using a suitable tool.	-	3	3	-	3	-	-	-	2	2

b. Course Assessment Matrix

Course Outcomes		Target							Program Outcomes Attained
		CIE				ESA	% students above Threshold	Threshold	
		Demo	Exercise	Str. Enquiry	Open Ended				
18ECSP202.1	Design and implement combinational and sequential circuits	-	✓	✓	-	✓	70	70%	PO1 - H PO3-M PO5-M
18ECSP202.2	Design and implement basic computer building blocks.	-	✓	✓	-	✓	65	70%	PO1 - H PO3-M PO5-M

18ECSP202.3	Simulate computer building blocks using a suitable tool.	-	-	✓	-	✓	65	70%	PO2 - H PO3-H PO5-H PO9-M PO10-M

c. Course Assessment Report

Course Name	PO1		PO2		PO3		PO5		PO9		PO10	
	ESE	ISA	ESE	ISA	ESE	ISA	ESE	ISA	ESE	ISA	ESE	ISA
18ECSP202.1	0	3	-	-	0	3	0	3	-	-	-	-
18ECSP202.2	0	3	-	-	0	3	0	3	-	-	-	-
18ECSP202.3	-	-	0	3	0	3	0	3	0	3	0	3
18ECSP202	**0**	**3**	**0**	**3**	**0**	**3**	**0**	**3**	**0**	**3**	**0**	**3**
Direct Assessment Total	0	2.61	0	2.5	0	2.5	0	3	0	3	0	3

5. Course Activity details for a team

TEAM NO: 2		
Name	USN	Roll No.
Raj Jain	01FE18BCS002	02
Aashish Kushwaha	01FE18BCS004	04
Aditya Anand	01FE18BCS016	16
Amit Singh Patel	01FE18BCS032	32

a. Problem Statement:

Design a datapath for the following data transfer instructions:

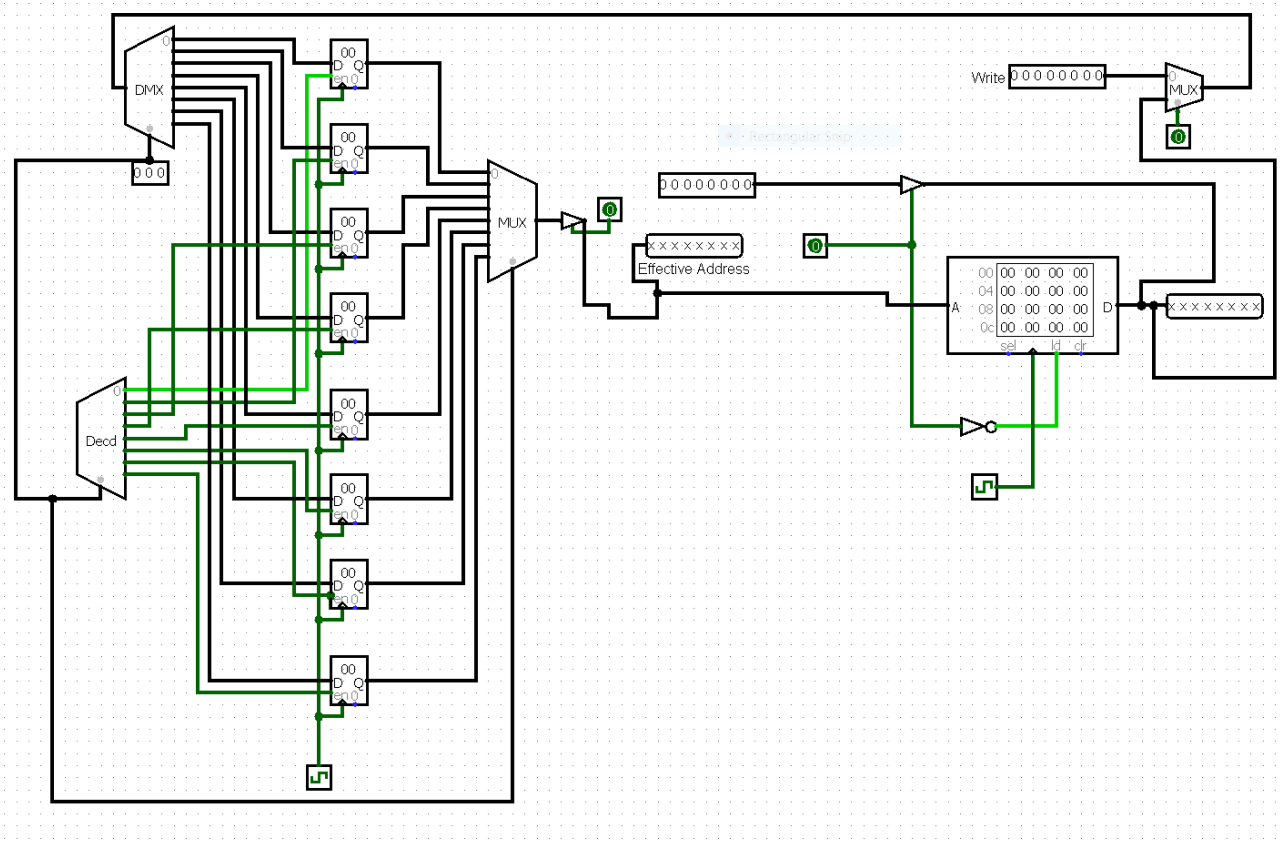
1) LOAD R4,(R6)
2) STORE R4,X(LOC)

b. Instruction Execution actions for LOAD:

- Fetch the instruction from the memory.
- Increment the program counter.
- Decode the instruction to determine the operation to be performed.
- Read register R6.

- Use the [R6] as the address of the source operand, and read the contents of that location in the memory.
- Load the data received from the memory into the destination register, R4.

c. Circuit diagram for LOAD instruction:



d. Instruction Execution actions for STORE:

- Fetch the instruction and increment the program counter.
- Decode the instruction and read registers R4 and LOC.
- Compute the effective address X + [LOC].

- Store the contents of register R6 into memory location X + [LOC].
- No action

e. Circuit diagram for STORE instruction